kontron

» DIGITAL-LOGIC AG is now a Kontron company «

Detailed USER MANUAL FOR:

SmartModule Express SMX945 / SMX945B



Converted Manuals are in Progress »

Including Specifications for: COMexpress SMX945

Nordstrasse 11/F
CH - 4542 Luterbach
Tel.: ++41 (0)32 681 58 00
Fax: ++41 (0)32 681 58 01
Homepage: http://www.digitallogic.com
Support: http://support.kcc-ag.ch

For internal use only:

File: SMX945_Detailed_V1.1.doc
Path: R:\HANDBUCH\smart\SMX945\SMX945_Detailed_V1.1.doc

About this Manual and How to Use It

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MICROSPACE-PC. It is for integrators and programmers of systems based on the MICROSPACE-Computer family. This manual provides instructions for installing and configuring the board, and describes the system and setup requirements. This document contains information on hardware requirements, interconnections, and details of how to program the system. Please check the Product CD for further information and manuals.

REVISION HISTORY:

Document Version	Date/Initials:	Modification: Remarks, News, Attention:
V1.0	05.2007 KUF	Initial Version
V1.0A	07.2007 KUF/WAS	Added: Schematics / Assembly-Disassembly Section / Updated Block Diagram / General corrections
V1.0B	09.2007 DAR/WAS	Attaching non-KCC heat sink (Sections 6.1 / 6.2.1)
V1.0C	10.2007 DAR	Chapter 6.1.7
V1.0D	01.2008 WAS	Sections 1.12 / 1.13 added
V1.0E	02.2008 DAR	Chapter 6
V1.0F	05.2008 KUF	Various additions / SMX945B spec. & picture
V1.0G	02.2009 WAS/SEP	LVDS channels Features & Flat Panel Interface Specs corrected
v1.1	***05.2011 WAS***	***Kontron logo & conversion to Kontron CI info added to title page.***

Attention!

1. All information in this manual, and the product, are subject to change without prior notice.
2. Read this manual prior to installation of the product.
3. Read the security information carefully prior to installation of the product.

Table of Contents

1. PREFACE

The information contained in this manual has been carefully checked and is believed to be accurate; it is subject to change without notice. Product advances mean that some specifications may have changed. Kontron AG assumes no responsibility for any inaccuracies, or the consequences thereof, that may appear in this manual. Furthermore, Kontron AG does not accept any liability arising from the use or application of any circuit or product described herein.

1.1. Trademarks

MICROSPACE®, smartModule®, smartCore®Express and DIGITAL-LOGIC® are trademarks or registered trademarks of Kontron Compact Computers AG. Kontron is a trademark or registered trademark of Kontron AG. In addition, this document may include names, company logos, and registered trademarks which are, therefore, proprietary to their respective owners.

1.2. Disclaimer

Kontron Compact Computers (KCC) makes no representations or warranties with respect to the contents of this manual, and specifically disclaims any implied warranty of merchantability or fitness, for any particular purpose. KCC shall, under no circumstances, be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage.

1.3. Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.4. Who should use this Product

- Electrical engineers with know-how in PC-technology.
- Because of the complexity and the variability of PC-technology, we cannot guarantee that the product will work in any particular situation or set-up. Our technical support will try to help you find a solution.
- Pay attention to electrostatic discharges; use a CMOS protected workplace.
- Power supply must be OFF when working on the board or connecting any cables or devices.

1.5. Recycling Information

All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered with a lead free process.

1.6. Technical Support

1. Contact your local Kontron Technical Support, in your country.
2. Use the Internet Support Request form at http://support.kcc-ag.ch/ → embedded products → New Support Request

Support requests are only accepted with detailed information about the product (i.e., BIOS-, Board-version)!

1.7. Limited Two Year Warranty

Kontron Compact Computers (KCC) guarantees the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for two years following the date of shipment from Kontron Compact Computers, Switzerland. This warranty is limited to the original purchaser of the product and is not transferable.

During the two year warranty period, Kontron Compact Computers will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to KCC. All replaced parts and products become property of KCC.

Before returning any product for repair, direct customers of Kontron Compact Computers AG Switzerland are required to register a RMA (Return Material Authorization) number in the Support Center at
http://support.kcc-ag.ch/

All other customers must contact their local distributors for returning defective materials.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by Kontron Compact Computers or other contingencies beyond the control of KCC), wrong connection, wrong information or as a result of service or modification by anyone other than Kontron Compact Computers. Nor if the user has insufficient knowledge of these technologies or has not consulted the product manuals or the technical support of KCC and therefore the product has been damaged.

Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer’s limited warranty.

Except, as directly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and Kontron Compact Computers expressly disclaims all warranties not stated herein. Under no circumstances will KCC be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

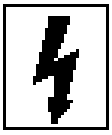
1.8. Explanation of Symbols



CE Conformity
This symbol indicates that the product described in this manual is in compliance with all applied CE standards.



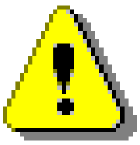
Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.



Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 32V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment



Warning, ESD Sensitive Device!
This symbol and title inform that electronic boards and their components are sensitive to Electro Static Discharge (ESD). In order to ensure product integrity at all times, care must always be taken while handling and examining this product.



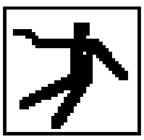
Attention!
This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your equipment.



Note...
This symbol and title emphasize aspects the user should read through carefully for his, or her, own advantage.



Warning, Heat Sensitive Device!
This symbol indicates a heat sensitive component.



Safety Instructions
This symbol shows safety instructions for the operator to follow.



This symbol warns of general hazards from mechanical, electrical, and/or chemical failure. This may endanger your life/health and/or result in damage to your equipment.

1.9. Applicable Documents and Standards

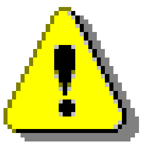
The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.htm
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems–Local and metropolitan area networks–Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 GB/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI-104 Specification, Version V1.0, November 2003. All rights reserved. http://www.pc104.org
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc, Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/

- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, Power-Smart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc., Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

1.10. For Your Safety

Your new Kontron Compact Computers (KCC) product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long, fault-free life. However, this life expectancy can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and for the correct operation of your new KCC product, please comply with the following guidelines.



Attention!
All work on this device must only be carried out by sufficiently skilled personnel.



Caution, Electric Shock!
Before installing your new KCC product, always ensure that your mains power is switched off. This applies also to the installation of piggybacks or peripherals. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltage before performing work.



Warning, ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. In order to ensure product integrity at all times, be careful during all handling and examinations of this product.

1.11. RoHS Commitment

Kontron Compact Computers is committed to develop and produce environmentally friendly products according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on July 1, 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for collection, recycling and recovery of electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union member state is adopting its own enforcement and implementation policies using the directive as a guide. Therefore, there could be as many different versions of the law as there are states in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California may have their own regulations for green products, which are similar, but not identical, to the RoHS directive.

RoHS is often referred to as the "lead-free" directive but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above mentioned substances is 0.1% (except for Cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component but to any single substance that could (theoretically) be separated mechanically.

1.11.1. RoHS Compatible Product Design

All Kontron Compact Computers (KCC) standard products comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all KCC standard products.

1.11.2. RoHS Compliant Production Process

Kontron Compact Computers selects external suppliers that are capable of producing RoHS compliant devices. These capabilities are verified by:

1. A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
2. If there is any doubt of the RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

1.11.3. WEEE Application

The WEEE directive is closely related to the RoHS directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company that brings the product to market, as defined in the directive. Components and sub-assemblies are not subject to product compliance. In other words, since Kontron Compact Computers does not deliver ready-made products to end users the WEEE directive is not applicable for KCC. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

1.12. Swiss Quality

- 100% Made in Switzerland
- This product was ***not*** manufactured by employees earning piecework wages
- This product was manufactured in humane work conditions
- All employees who worked on this product are paid customary Swiss market wages and are insured
- ISO 9000:2001 (quality management system)

1.13. The Swiss Association for Quality and Management Systems

The Swiss Association for Quality and Management Systems (SQS) provides certification and assessment services for all types of industries and services. SQS certificates are accepted worldwide thanks to accreditation by the Swiss Accreditation Service (SAS), active membership in the International Certification Network, IQNet, and co-operation contracts/agreements with accredited partners.

www.sqs.ch

The SQS Certificate ISO 9001:2000 has been issued to Kontron Compact Computers AG, the entire company, in the field of development, manufacturing and sales of embedded computer boards, embedded computer modules and computer systems. The certification is valid for three years at which time an audit is performed for recertification.

2. OVERVIEW

2.1. Standard Features

The smartModuleExpress945 is a miniaturized PC system on chip unit incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

- Powerful Core Duo, Core 2 Duo, Core Solo CPU
- DDR2 SODIMM socket for 256MByte to 2GByte (SMX945), RAM-Module
- 1GB DDR2 RAM soldered onboard, only SMX945B
- DDR2 SODIMM socket for 256MByte to 2GByte RAM-Module (SMX945B max. 3GB RAM)
- Dual 220pin connectors (1st Connector: Rows A-B and 2nd Connector: Rows C-D, 440pins total)
- COMexpress Bus Type 2
- 32bit PCI interface
- IDE port (to support legacy ATA devices as CD-ROM and CompactFlash)
- Up to 6 PCI Express general purpose lanes
- One, 1x16 PCI Express Graphics (PEG) slot
- SDVO option (pins shared with PCI Express Graphics)
- Maximum module input power capability extended to 80W
- Maximum Thermal Design Power up to 40W
- Up to 8 USB 2.0 ports; 4 shared over-current lines
- Up to 2 Serial ATA ports
- Dual 24bit LVDS channels
- Analog VGA
- Powerful internal Graphic controller GMA950
- Intel High Definition Audio (Azalia) and AC '97 digital audio interface (external CODEC)
- Single Ethernet interface 100/10Mbit/s with integrated PHY
- AMI BIOS
- LPC Bus for SuperIO (COM1/2, LPT, FD), diagnostics, BIOS device

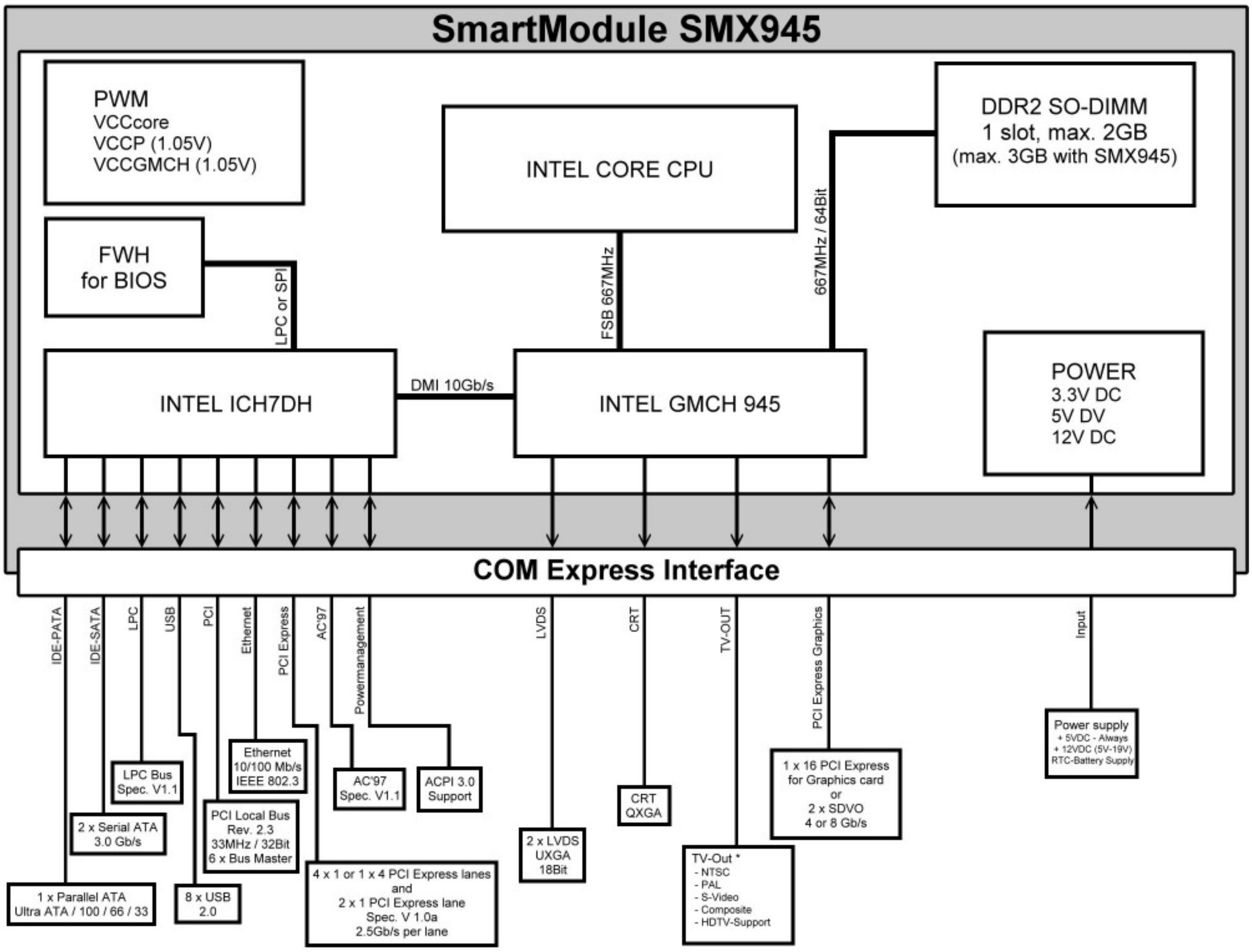
2.2. Unique Features

- EEPROM for setup and configuration
- UL approved parts
- Remote Function
- Thermal Interface with a very low thermal resistance (copper core)
- Very ruggedized, withstands highest mechanical vibration and shock
- Very low power consumption → no active cooling required
- Extended wide range power input for single 5Volt supply applications
- Power Management Microcontroller

2.3. Standards

Specification	Location
Low Pin Count Interface Specification, Revision 1.0 (LPC)	http://developer.intel.com/design/chipsets/ industry/lpc.htm
Audio Codec '97 Component Specification, Version 2.3 (AC '97)	http://developer.intel.com/ial/ scalableplatforms/audio/index.htm
Wired for Management Baseline, Version 2.0 (WfM)	http://www.intel.com/labs/manage/wfm/ index.htm
System Management Bus Specification, Version 2.0 (SMBus)	http://www.smbus.org/specs/
PCI Local Bus Specification, Revision 2.2 (PCI)	http://pcisig.com/specifications.htm
AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6) Specification	http://www.t13.org
Universal Serial Bus (USB) Specification, Revision 2.0	http://www.usb.org
Advanced Configuration and Power Interface (ACPI) Specification, *Revision 2.0*	http://www.acpi.info
Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0	http://developer.intel.com/technology/usb/ ehcispec.htm

2.4. Block Diagram



* This function is disabled.
A Macrovision license is required to enable it.
(only with GM chipset / GME chipset does not support Macrovision)

2.5. Specifications

CPU	Specification
CoreDuo / Celeron M	Intel Core Duo L2400 LV 2x 1.66GHz with 2MB L2-cache Intel Core 2 Duo L7400 LV 2x 1.66GHz with 4MB L2-cache
Clock	1GHz up to 1.86GHz
1st Level Cache	2x 32kByte
2nd Level Cache	1, 2, 4 MByte (on die)
Technology	65nm
VCCCore @ 1.6GHz	1.308V
VCCCore @ 0.6GHz	0.844V
VCCCore @ deep sleep	0.748V
CPU-Bus	AGTL+
AGTL+ Termination	Integrated
FSB	533/666MHz quad-pumped synchronous bus

Mathematics Coprocessor	
	Available on the PENTIUM CPU

Intel 945GME Graphics Memory Controller Hub	
Memory Controller	**Specification**
Supports	PC1600 / PC2100 / PC2700
Socket	DDR2 SODIMM 200pin (SMX945B 1GB soldered on board)
Technologies	DDR2-667
Capacity	256MByte up to 2GByte (3GByte with SMX945B)
Voltage	2.5V
Termination	1.25V
Width	64bit
ECC-Support	No

Intel 945GME Graphics Memory Controller Hub	
Graphic Controller Alternative to the PEG Interface	**Specification**
Max. Video memory	224MByte with Intel GMA950
Graphic Core Frequency	400MHz
3D Graphic Engine	3D-setup and rendering engine Zone rendering Texture engine
Direct-X Compatibility	Direct-X9
Analog CRT	400MHz RAMDAC with 24bit Resolution up to 2048 x 1536 @ 70Hz (QXGA) Hardware cursor support I2C and DDC channels Dual independent display
SDVO Port	2 channels (multiplexed with the PEG signals) 2x 200 Mpixel/sec Support for up to 2x DVI, 1x TV and 2x LVDS Dotclock = 165MHz Compliant with DVI Spec.1.5
Flat Panel Interface	2 channel LVDS interface 1x 18, 2x 18, 1x24, 2x24bpp TFT Dotclock = up to 2x 112 MHz Resolutions 640 x 480 up to 1600 x 1200 (UXGA) Automatic panel detection via VESA EDID 1.3
TV Out	Disabled. A Macrovision license is required.

Intel 945GME Graphics PEG	
PEG Controller Alternative to the internal graphic controller multiplexed with the SDVO signals	**Specification**
Support	PEG
Mode	16 lanes
Voltage	1.5Volt
Signals	Differential 2.5Gbit/sec

Intel 82801DBM (ICH7DH)	Specification
PCI-Bus	Supports PCI 2.2 with 6 resources
EIDE-Bus	1x Ultra P-ATA 100
SATA-Bus	2 channels 150MByte/sec
USB V2.0	8 channels USB
APIC	INTEL I/O APIC
SMB	V2.0 SMBus controller
FWH	Firm Ware Hub for BIOS devices
LPC	Serialized BUS (no ISA) used for external SuperIO (COM1/2, MS, KB, FD and LPT)
Sound	AC97 2.3 HDA Interface with 192kHz sampling rate and 8 channels
IRQ Controller	8259 compatible
Timers	8254 compatible
Power Management	Integrated

Reset & Power Management	Specification
Controller	PIC 16C870
Power Modes	S5, S4, S3, S1
ACPI	V3.0

BUS	Specification
PCI	PCI 2.2 33MHz 32bit
LPC	8bit 33MHz
PCIexpress	6x 1 lane, PEG

Power Supply	Specification
DC Input	5.0V up to maximum 18V, max. 200mV ripple up to 30 Watts peak for VCCCore, 2.5V and 1.25V generation
Inrush current	5.0V up to 10Amp for 100µs ★ 18.0V up to 30Amp for 20µs ★
5.0Volt	0.1Amp (VCC5ALW)
Onboard Voltages	VCC-Core, 1.05V, 1.2V, 1.25V, 1.3V, 1.5V, 1.8V, 2.5V, 3.3V
Power Consumption	800MHz: approx. 6Watts @ 512MByte DDR2-RAM, Desktop load 1.6GHz: approx. 24Watts @ 512MByte DDR2-RAM, 100% workload

★ Use inductors in series to reduce the maximum inrush current!

Physical Characteristics	Specification
Dimensions	Length: 117 mm +/- 0.1mm Depth: 70 mm +/- 0.1mm Height: 15 mm +/- 0.2mm (with 5mm bus connectors) 18 mm +/- 0.2mm (with 8mm bus connectors) The connector height is selected by the connector on the carrier board.
Weight	120 grams / 12 ounces
PCB Thickness	1.6 mm / 0.0625 inches nominal
PCB Layer	Multilayer

Operating Environment	Specification
Relative Humidity	5-90% non-condensing
Vibration	5 to 2000 Hz
Shock	10 G
Operating Temperature	Standard: T.B.D. (depends on the CPU and the cooling concept) Extended Range: T.B.D.
Maximum Copper Temperature	90℃
Storage Temperature	-55℃ to +85℃

EMI / EMC (IEC1131-2 refer MIL 461/462)	Specification
ESD Electro Static Discharge	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 Metallic protection needed Separate Ground Layer included 15 kV single peak
REF Radiated Electromagnetic Field	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. Not tested
EFT Electric Fast Transient (Burst)	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1KV Supply, 500 I/O, 5Khz
SIR Surge Immunity Requirements	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2kV, 6 pulse/minute I/O: 500V, 2 pulse/minute FD, CRT: None
High-Frequency Radiation	EN55022

All information is subject to change without notice.

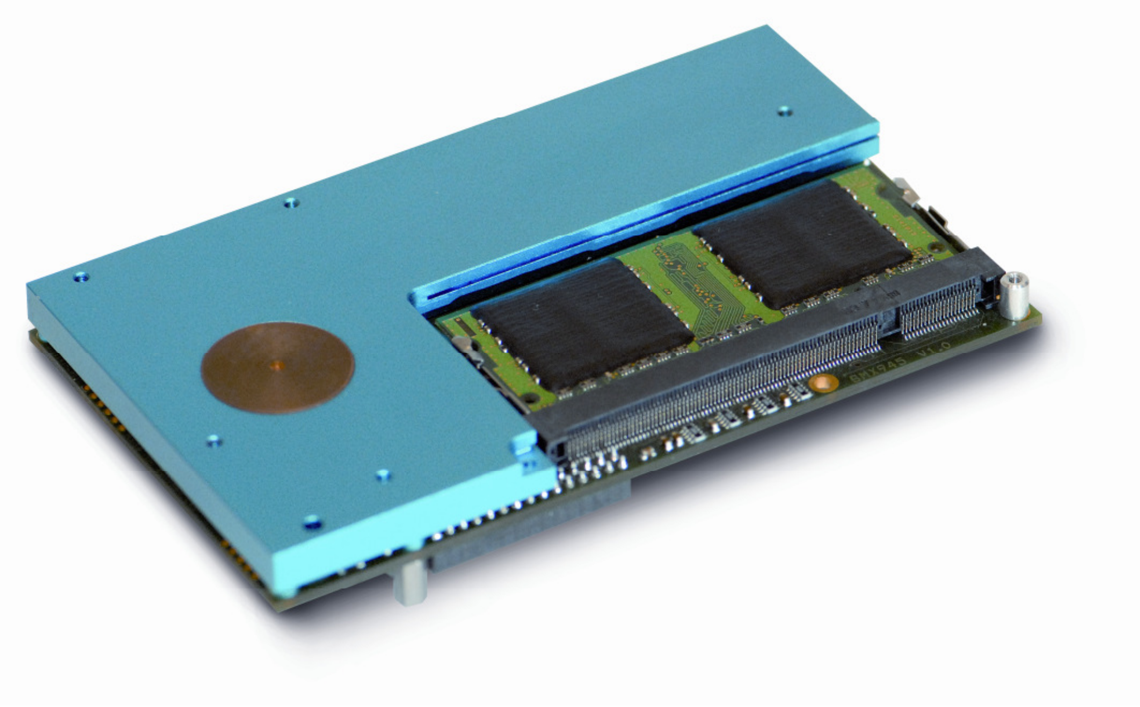
2.6. Examples of Ordering Codes

Product Name	Part Number	Description
SMX945-L2400	805350	smartModuleExpress945, Core Duo L2400, 0MB RAM
SMX945-L7400	805352	smartModuleExpress945, Core 2 Duo L7400, 0MB RAM

These are only examples; for current ordering codes, please see the current price list.

2.7. Product Pictures:

2.7.1. SMX945:



2.7.2. SMX945B



2.8. Thermoscan

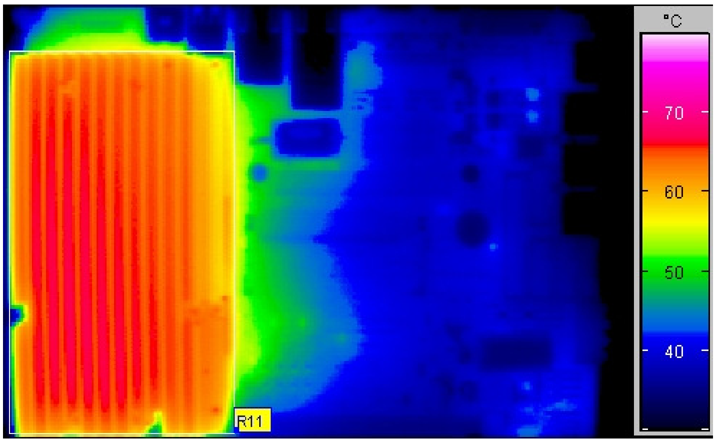
2.8.1. SMX945 – CPUs

CPU with 512MB-RAM	Desktop WIN-XP	100% workload	Standby
Core Duo L7400	1.2A / 6W	4.4A / 22W	1.4A / 7W
Core Duo L2400	1.2A / 6W	4.8A / 24W	1.4A / 7W
Celeron M 423	1.4A / 7W	2.5A / 13W	1.4A 7 7W
Celeron M 440	1.9A / 10W	4.6A / 23W	1.4A / 7W

2.8.2. SMX945-L2400 (mounted on EBX-Board)

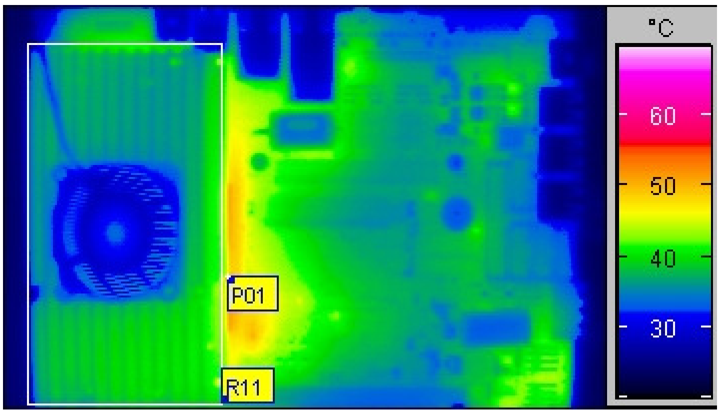
Product	Part Number	Serial Number	Version
MSEBX945			
SMX945-L2400			
SODIMM DDR2 512MB			
Software:	After INT 19 (before starting OS)		

MSEBX945 passive cooled – Top View



t [min]	f_{CPU} [MHz]	I [mA]	R11[°C]	VCC[V]
60	2000	2500	66.8	12

MSEBX945 active cooled – Top View



t [min]	f_{CPU} [MHz]	I [mA]	R11[°C]	P01[°C]	VCC [V]
60	2000	2500	45.9	51.7	12

3. PC FUNCTIONAL DESCRIPTION

3.1. Power Input

The SMX945 module uses a single main power rail with a nominal value of +12V. Kontron Compact Computers has expanded the 12Volt input to a wide-range input, working between 5Volt and 18Volt.

Main supply: 5.0Volt (-0.1V) to 18Volt (+0V) with 20-30Watt depending on the processor.

The sources of the main supply may be:

- 12Volt supply as the COMexpress Specs define
- Single 5Volt systems such as PC/104express
- Battery supplied systems (Li-ion with 14.4Volt nominal)
- Vehicle supply, nominal with 12V

Two additional voltage inputs are specified:

- +5V Always (0.1Amp) = VCC_5V_SBY = VCC5ALWAYS
- +3V-3.6V battery input to power the module Real-time Clock (RTC) circuit

3.1.1. Power Supply Sequencing

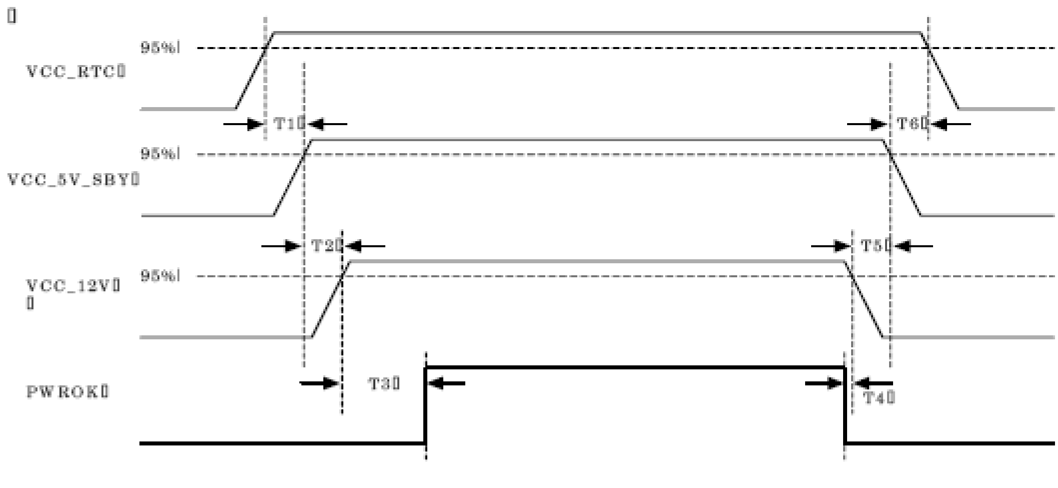


Table 7-3: Power Sequencing

T1	VCC_RTC rise to VCC_5V_SBY rise	≥ 0 ms
T2	VCC_5V_SBY rise to VCC_12V rise	≥ 0 ms
T3	VCC_12V rise to PWROK rise	≥ 0 ms
T4	PWROK fall to VCC_12V fall	≥ 0 ms
T5	VCC_12V fall to VCC_5V_SBY fall	≥ 0 ms
T6	VCC_5V_SBY fall to VCC_RTC fall	≥ 0 ms

3.1.2. Battery Backed Clock (RTC)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

Connect an external Lithium battery of 3.0V-3.6V to the RTC pin.

The battery-backed clock can be set by using the Kontron Compact Computers SETUP at boot-time.

Addresses: 70h = Index register
71h = Data transfer register

RTC-Address MAP: 00-0F Real time clock
10-3F BIOS setup (Standard)
40-7F Extended BIOS

Voltage range: 2.0-3.6V DC

With an external Lithium 3.6V / 400mAh battery, the board will work for over 10 years without needing a replacement battery. The chipset consumes the following currents:

Typical battery current at 25°C: 2.4uA @ typ. 3V DC

3.1.3. Watchdog

The watchdog timer detects a system crash and performs a hardware reset. After power up, the watchdog is always disabled as the BIOS does not send strobes to the watchdog. In case that the user wants to take advantage of the watchdog, the application must produce a strobe at least every 800 ms. If no strobe occurs within the 800 ms, the watchdog resets the system.

For more information, please refer to the driver/software/BIOS manual SMX945_BIOS on the Product CD. The watchdog feature is integrated in the INT15 function.

There are some programming examples available:
Product CD-Rom or customer download area: \tools\SMX945\int15dl\...

3.2. Watchdog Control

Interface/Function	On the smartModule	Circuits needed on the OEM board
External WatchDOG Control	Standard – automatically strobed with 32kHz	

3.3. BIOS

3.3.1. ROM-BIOS

An EPROM with 8bit wide data access normally contains the board's AT compatible ROM-BIOS. The BIOS takes an E82802AC8 EPROM (or equivalent) device on the LPC-Bus. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this (socket). The ROM-BIOS occupies the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already usable for ROM-DOS and BIOS expansion modules.

Consult the appropriate address map for the MICROSPACE SMX945 ROM-BIOS.

Standard BIOS ROM

DEVICE: Intel E82802AC8 onboard soldered

MAP:	E0000 - FFFFFh	Core BIOS, 1024kB
	C0000 - CFFFFh	VGA BIOS, 64kB

3.3.2. EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down and the checksum error would appear and stop the system. The capacity of the EEPROM is 2 kByte.

Organization of the 2048Byte EEPROMs:

Address MAP	Function
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Reserved**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**Reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial Number**
0110h-0113h	Production Date (year/day/month)
0114h-0117h	1st Service Date (year/day/month)
0118h-011Bh	2nd Service Date (year/day/month)
011Ch-011Fh	3rd Service Date (year/day/month)
0120h-0122h	Boot errors (Auto incremented if any boot error occurs)
0123h-0125h	Setup Entries (Auto incremented on every setup entry)
0126h-0128h	Low Battery (Auto incremented every time the battery is low, EEPROM→CMOS)
0129h-012Bh	Startup (Auto incremented on every power-on start)
0130h	Reserved
0131h	Reserved
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE: ('M'=PC/104, 'E'=Euro, 'W'=MSWS, 'S'=Slot, 'C'=Custom, 'X'= smartCore or smartModule)
0137h	CPU TYPE: (01h=ELAN300/310, 02h=ELAN400, 05h=P5, 08h=P3, 09h=Elan520, 10h=P-M)
0200h-03FFh	**Reserved**
0200h-027Fh	Reserved
0400h-07FFh	**Free for Customer's use**

3.4. CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64Bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128Bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain System BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

3.5. System Memory Map

The PENTIUM™ CPU, used as a central processing unit on the MICROSPACE, has a memory address space which is defined by 32 address bits. Therefore, it can address 4GBytes of memory. The memory address map is as follows:

CPU Pentium

Address	Size	Function / Comments
000000 - 09FFFFh	640kBytes	Onboard DRAM for DOS applications
0C0000 - 0CBFFFh 0CC000 - 0CFFFFh	48kBytes 16kBytes	VGA BIOS, selected by the hardware BIOS extensions, selected by the hardware
0D0000 - 0D4000h 0D4000 - 0D8000h 0D8000 - 0DFFFFh	16kBytes 16kBytes 32kBytes	Free for user Free for user Free for user
0E0000 - 0FFFFFh	1024kBytes	Core BIOS, selected by the 945GM chipset
100000 - 1FFFFFh	1MByte	DRAM for extended onboard memory
200000 - FFFFFFh	14MBytes	DRAM for extended onboard memory

3.6. Graphics Controller

The Intel 945GM Express Chipset

The GMCH IGD provides a highly integrated graphics accelerator delivering high performance 2D, 3D and video capabilities. With its interfaces to UMA using a DVMT configuration, an analog display, a LVDS port and two digital display ports (e.g. flat panel), the GMCH can provide a complete graphics solution.

The GMCH also provides 2D hardware acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2 and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks with the hardware reduces the CPU load and thus improves performance.

High bandwidth access to data is provided through the system memory interface. The GMCH uses tiling architecture to increase the system memory efficiency and thus maximize effective rendering bandwidth. The Intel 945GME GMCH also improves 3D performance and quality with 3D Zone Rendering technology.

The GMCH has four display ports, one analog and three digital. These provide support for a progressive scan analog monitor, a dedicated dual channel LVDS LCD panel, and two DVO devices. Each port can transmit data according to one or more protocols. The DVO ports are connected to an external device that converts one protocol to another. Examples of this are TV-out encoders, external DACs, LVDS transmitters and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device. The data that is sent out of the display port is selected from one of two possible sources, Pipe A or Pipe B.

3.6.1. Analog Display Port

The Intel 945GM GMCH has an integrated 400MHz, 24bit RAMDAC that can directly drive a progressive scan analog monitor pixel resolution of up to 1600x1200 at 85Hz refresh and up to 2048x1536 at 72Hz refresh. The analog display port can be driven by Pipe A or Pipe B.

3.6.2. Integrated LVDS Port

The Intel 945GM GMCH has an integrated dual channel LFP transmitter interface to support LVDS LCD panel resolutions up to UXGA with center and down spread SSC support of 0.5%, 1%, and 2.5% utilizing an external SSC clock. The display pipe provides panel up-scaling to fit a smaller source image onto a specific native panel size, as well as provides panning and centering support. The LVDS port is only supported on Pipe B. The LVDS port can only be driven by Pipe B, either independently or simultaneously with the Analog Display port.

3.6.3. Integrated DVO Ports

The DVO B/C interface is compliant with the DVI Specification 1.0. When combined with a DVI compliant external device (e.g. TMDS Flat Panel Transmitter, TV-out encoder, etc.), the GMCH provides a high-speed interface to a digital or analog display (e.g. flat panel, TV monitor, etc.). The GMCH provides two DVO ports that are each capable of driving a 165MHz pixel clock at the DVO B or DVO C interface. When DVO B and DVO C are combined into a single DVO port, then an effective pixel rate of 330MHz can be achieved. The DVO B/C ports can be driven by Pipe A or Pipe B. If driven on Pipe B, then the LVDS port must be disabled.

4. DESCRIPTION OF THE JUMPERS

Note…
There are no jumpers on this product!

5. LED CRITERIA:

LED	Color	Function
D26	Green	Run OK
D31	Green	3.3Volt OK

The Power & Control LEDs on the SMX945PC

There are 2 LEDs located on the top side of the smartModule:

1. The green Power LED

    a. Indicates that the 3.3V core supply for the CPU is OK.

    b. This LED must light as soon as the external 5V power supply is available.

2. The green Reset/Run LED

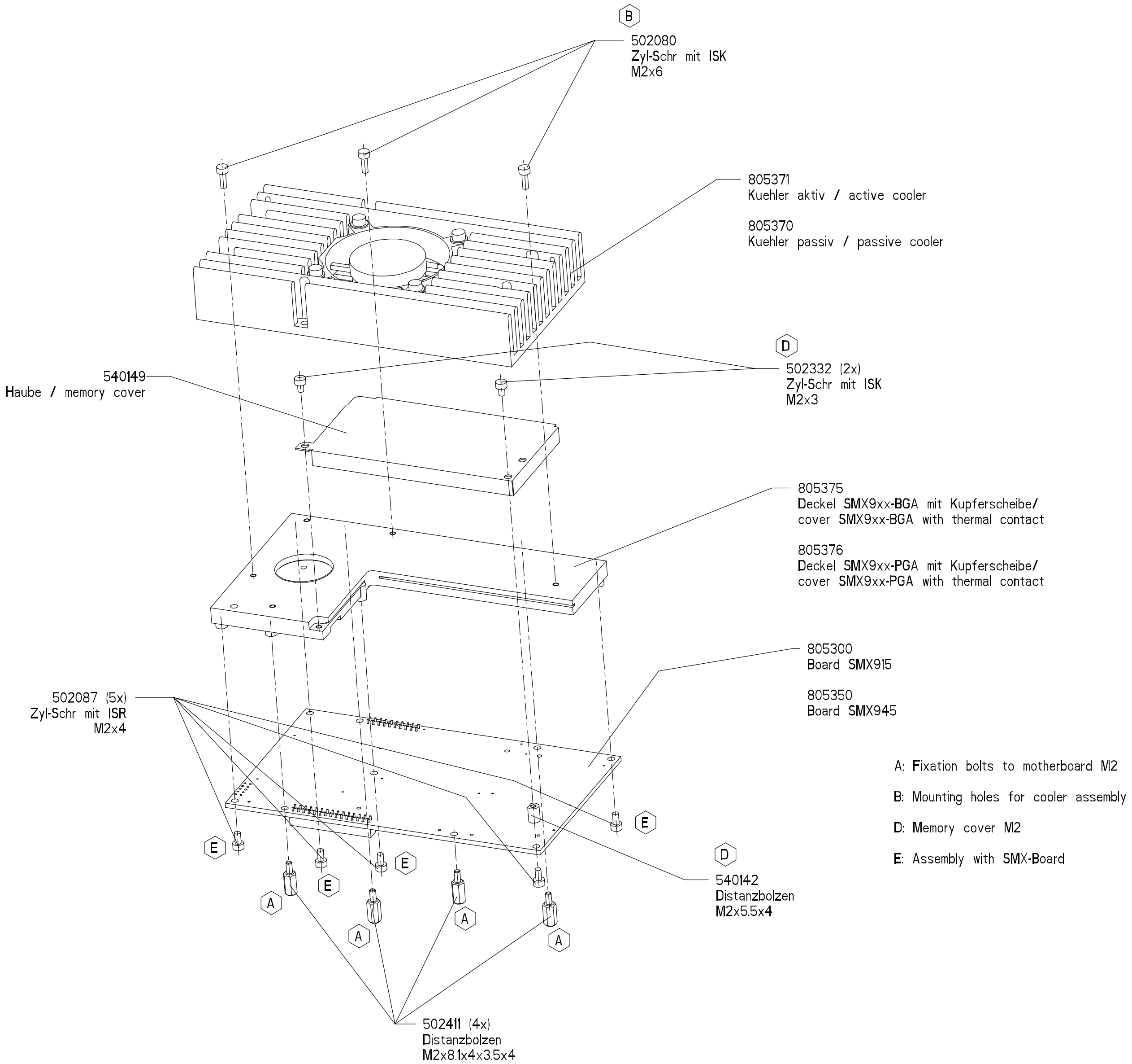
OFF: The module is in the Reset state which means there is no operation.
Either the Watchdog, the power supervisor or an active external reset signal holds the module in the Reset state.

ON: The module is running normally.
After power up, this LED must come ON after 1-2 seconds.

After a successful boot sequence, both green LEDs are on!

6. DESIGN-IN WITH THE SMARTMODULE

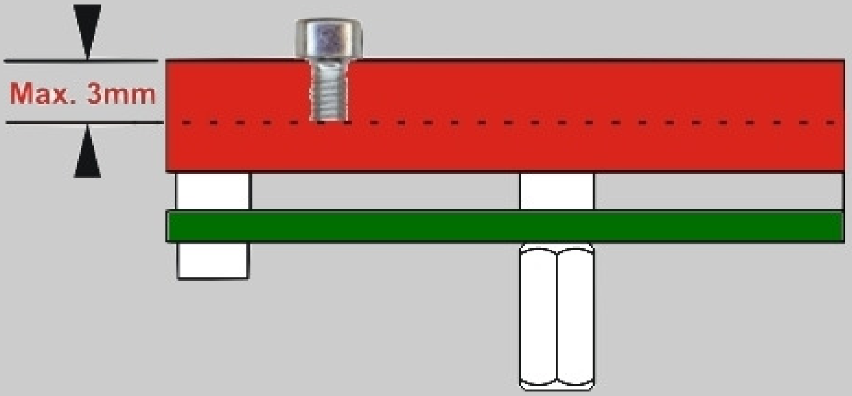
6.1. Mechanical Assembly



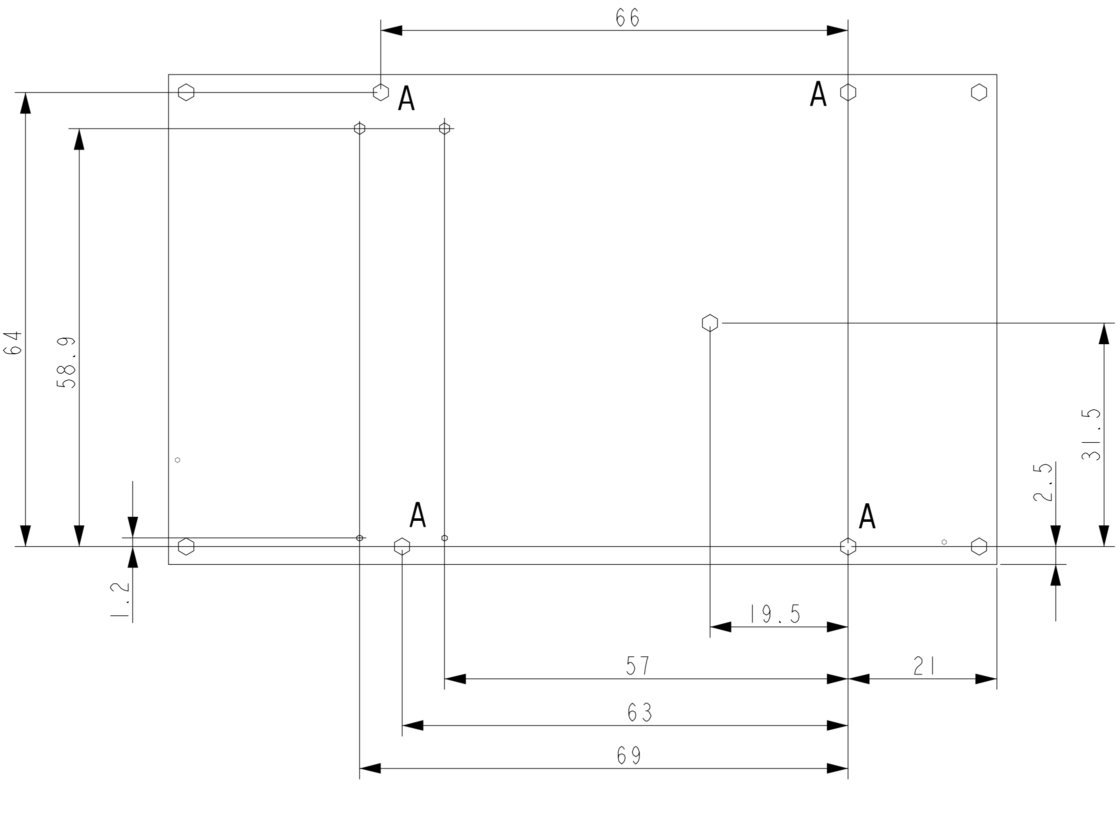
Attention!

When using an active/passive heatsink that is **not** from KCC, be very careful!

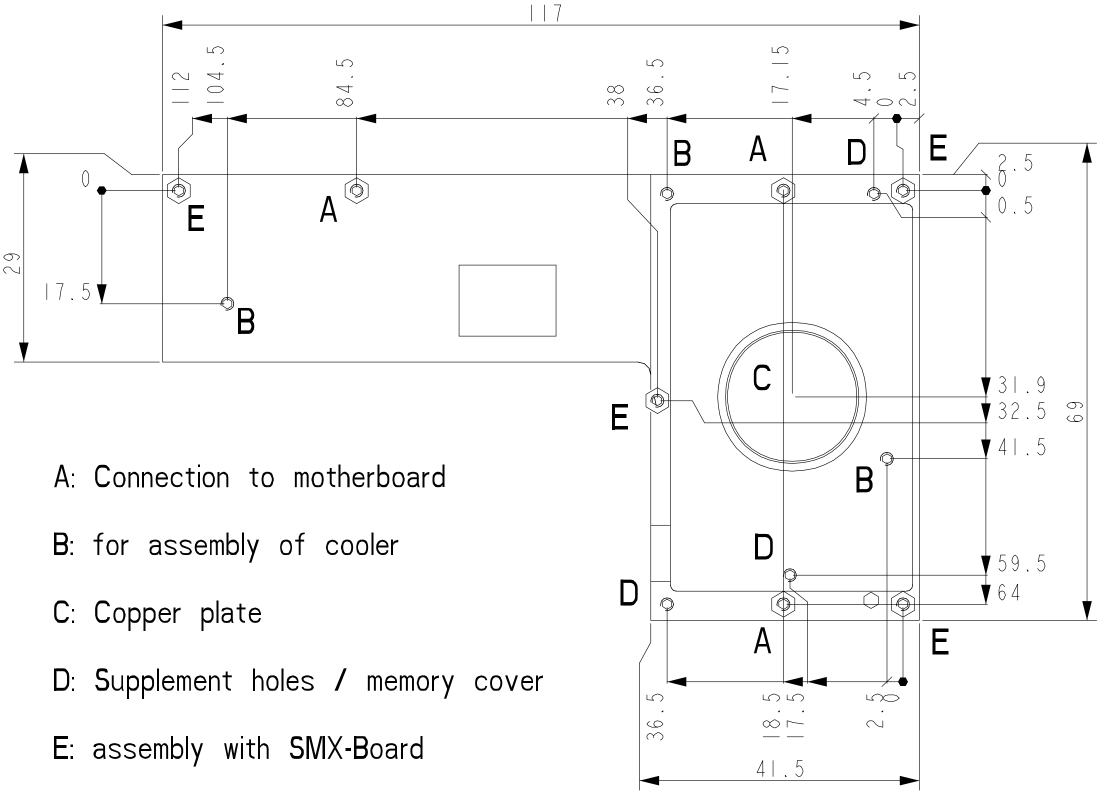
The maximum depth the screws can go into the product is 3mm or the smartModule will be destroyed!



6.1.1. Dimensions of the SMX945 Computer on Module



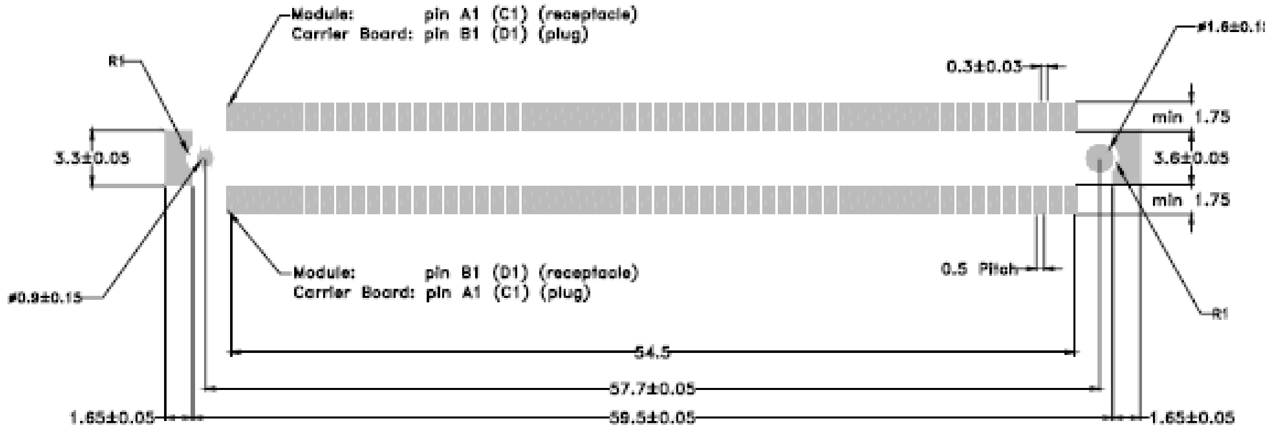
A = Fixation holes to motherboard M2



117
112
104.5
84.5
38
36.5
17.15
4.5
0
2.5
A
B
C
D
E
29
17.5
69
31.9
32.5
41.5
59.5
64
0.5
18.5
17.5
41.5
A: Connection to motherboard
B: for assembly of cooler
C: Copper plate
D: Supplement holes / memory cover
E: assembly with SMX-Board

6.1.2. Connector Placement & Pin Definition on the Carrier Board

Top View of the PCB:



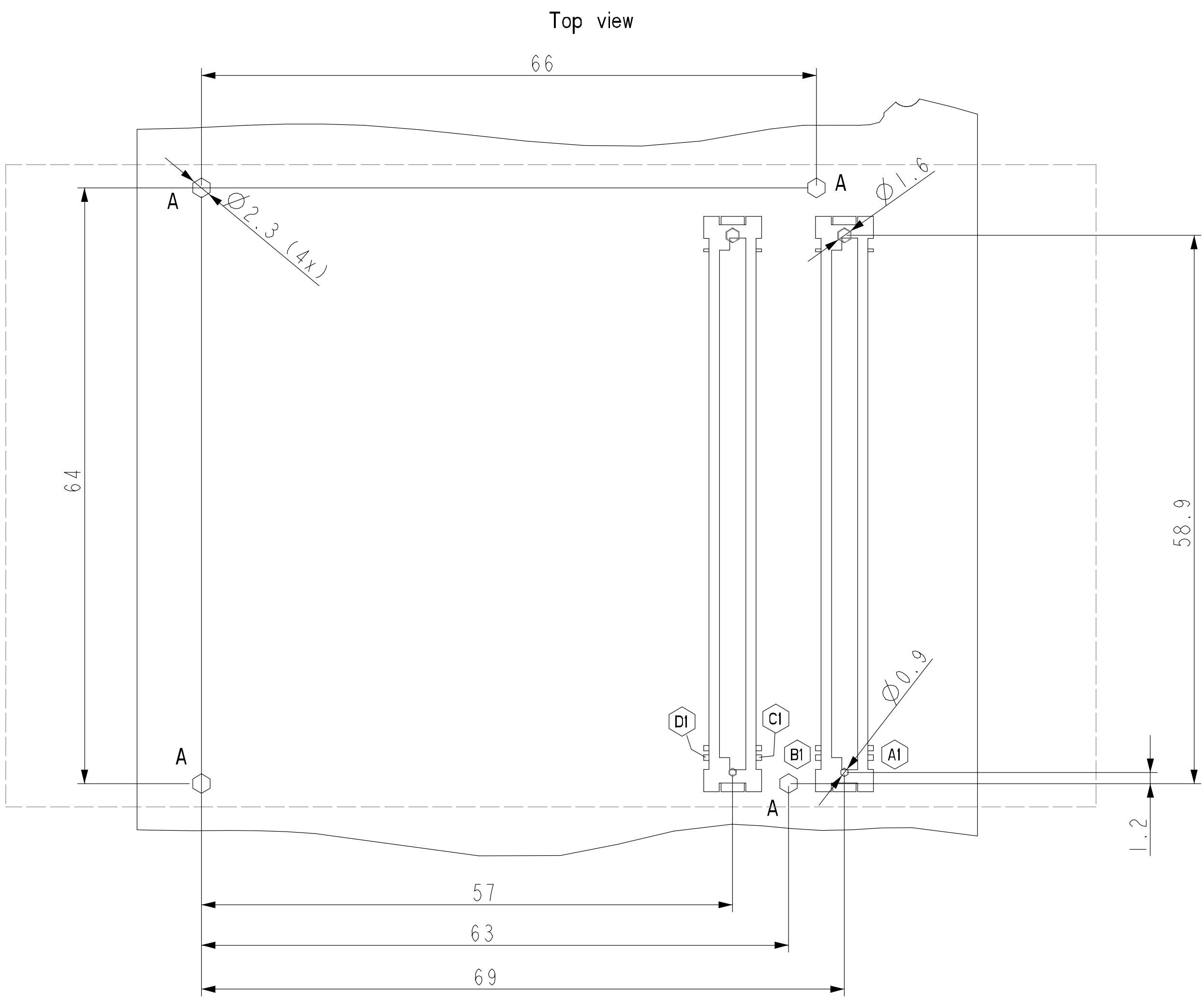
Remarks:

1. All dimensions in millimeters.
2. For the carrier board, use the Pin Definition A1/B1/C1/D1 for the plug.
3. The receptacle is mounted on the SMX945/915.

Top View, Pin Definition for the Carrier Board PCB:

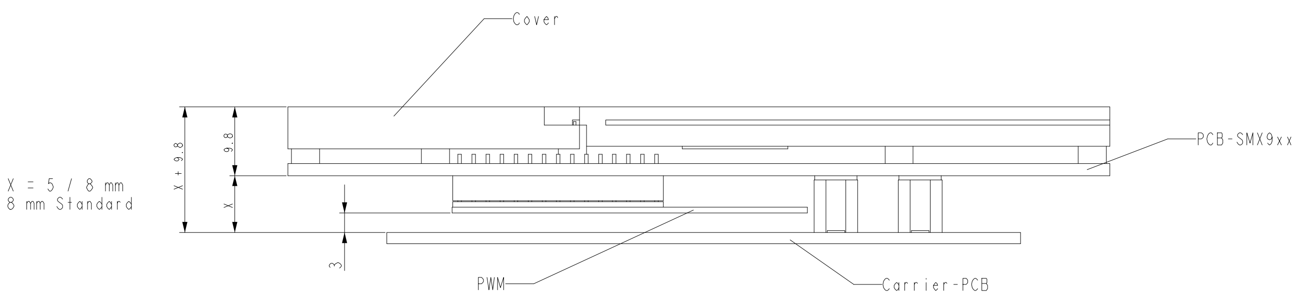


6.1.3. Connector Placement on the Carrier Board

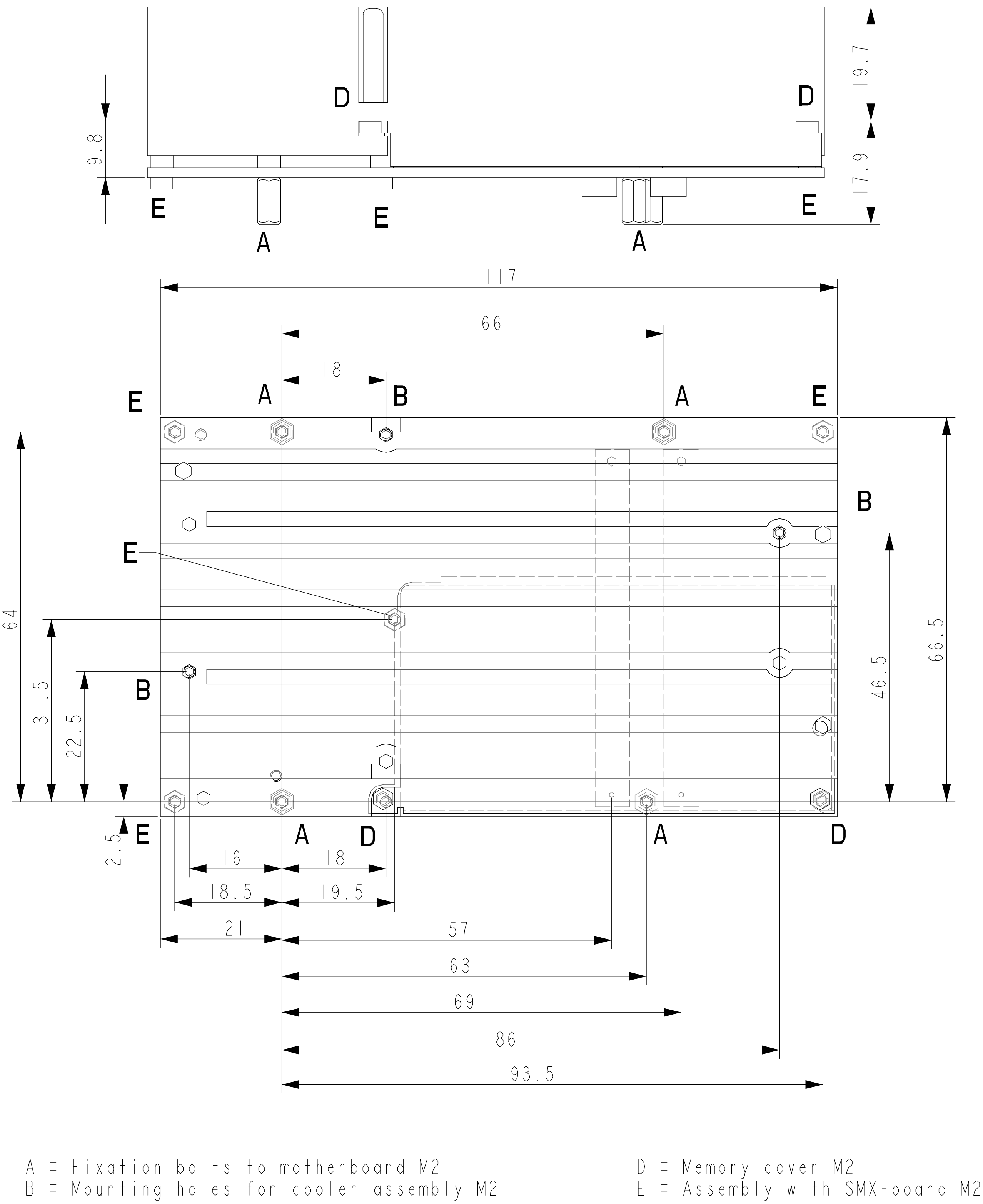


A : Fixation holes to motherboard M2

6.1.4. Height of the Module Stack



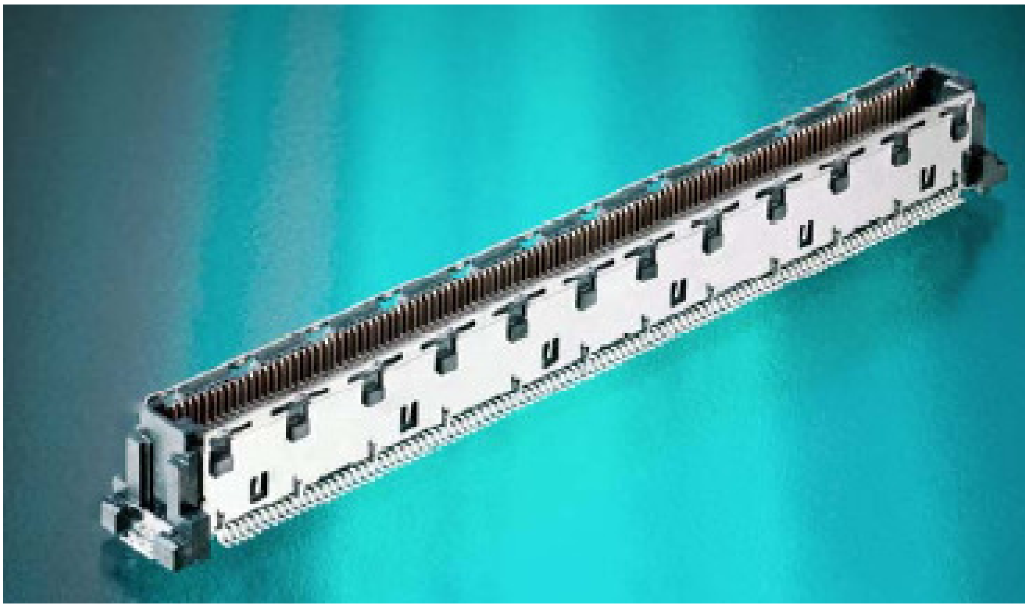
6.1.5. Mechanical Dimensions



6.1.6. Dimensions of the Carrier Board Connector

SMX-CON8:
Standard height: 8.0mm
KCC part number: 807138
AMP/Tyco: 8-6318491-6

(components placed below the smartModule total a maximum 2.0mm)

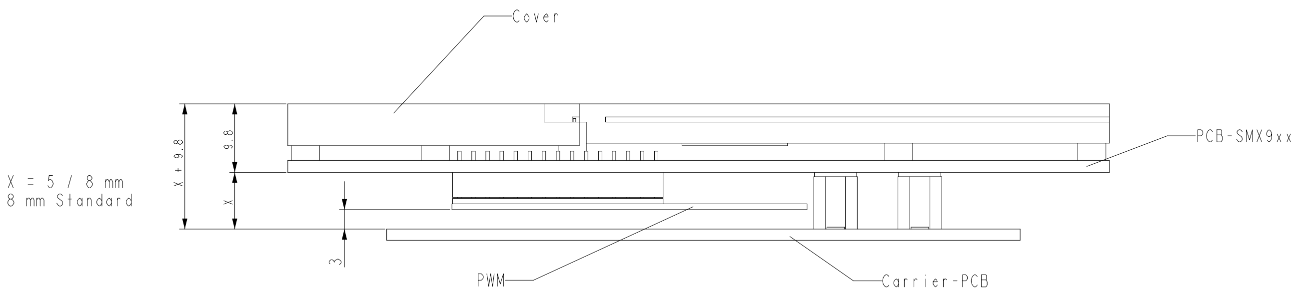


6.1.7. Component Heights between Module and Carrier Board

Parts mounted on the back side of the module (in the space between the bottom surface of the module PCB and the carrier board) should have a maximum height of 8.0mm.

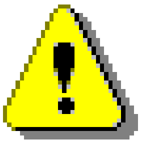
8mm stack height standard for SMX945:

If the carrier board uses the 8mm stack option, then the carrier board topside components within the module envelope are limited to a height of 1.6mm, with the exception of the mating connectors. Using carrier board topside components up to 1.6mm allows a gap of 0.4mm between the carrier board topside components and the module's bottom side components.



6.2. Assembly / Disassembly

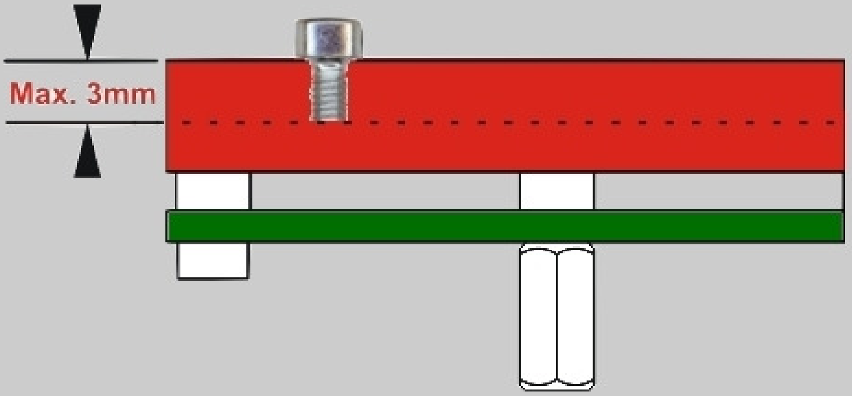
6.2.1. Passive/Active Heat Sink

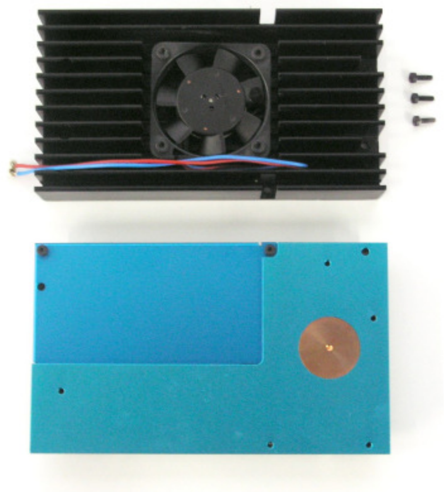
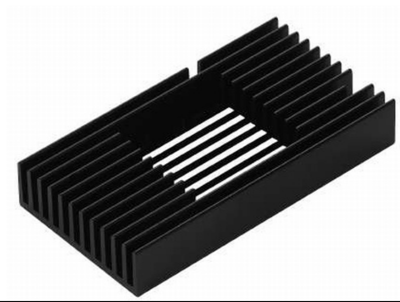
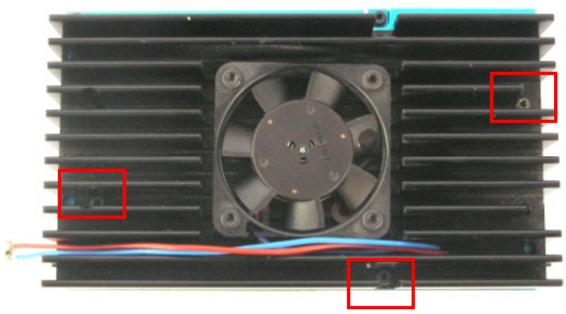


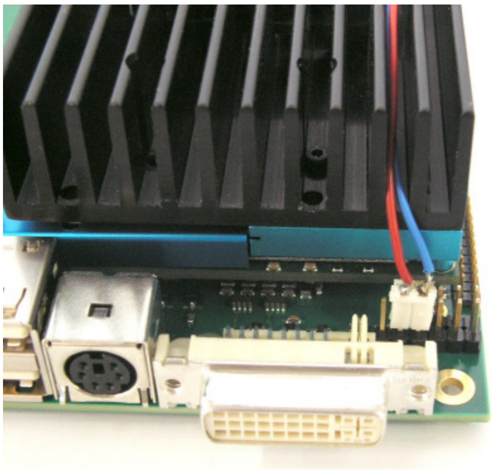
Attention!

When using an active/passive heatsink that is **not** from KCC, be very careful!

The maximum depth the screws can go into the product is 3mm or the smartModule will be destroyed!



	The photo on the left shows the basic SMX945 with active heat sink. The photo below shows a passive heat sink. Assembly is the same except Step 3 is not required for a passive heat sink. The passive heat sink has no electric connection. 
	**Step 1:** Put the active heat sink onto the SMX945. **Step 2:** Affix the heat sink with 3 screws. Screw type: Cylinder hexagon socket type screw M2x6mm / BN7 DIN 912 ISO 4762 Tool: Hexagon head socket wrench no. 1.5

<table>
<tr>
<td>
Pictured: electric connection on the MSEBX945.</td>
<td>Step 3:

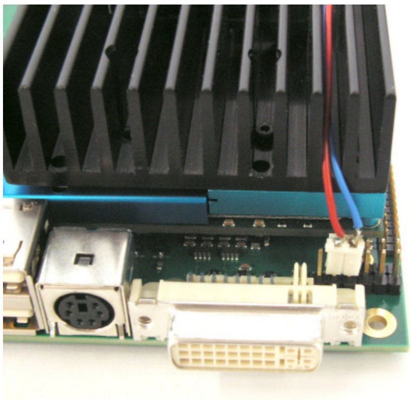
Plug the fan into the electric connection on the host board. For example:

On the MSEBX945 V1.0:

Connector X207 Pin1 (GND) and Pin2 (FAN1_PWR)
or
Connector X208 Pin1 (GND) and Pin2 (FAN2_PWR)

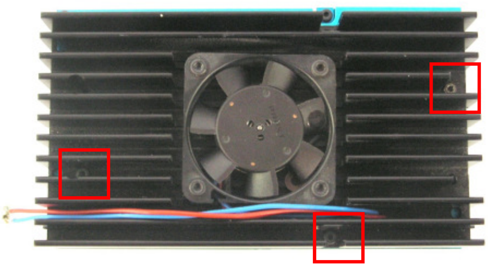
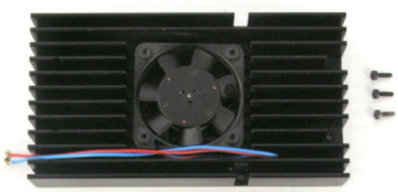
On the MSM945:
Connector X205</td>
</tr>
</table>

6.2.2. SODIMM-DDR2 RAM

<table>
<tr>
<td></td>
<td>Step 1:

In the case of an active heat sink, remove the electric fan connector.

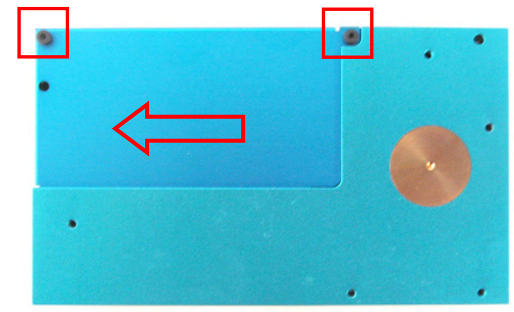
This step is not required for a passive heat sink.

(The photo shows the basic MSEBX945 board with active heat sink.)</td>
</tr>
<tr>
<td>

</td>
<td>Step 2:

Remove the 3 screws from the heat sink and dismantle the heat sink.

Screw Type: Cylinder hexagon socket type screw
M2x6mm / BN7 DIN912 ISO 4762

Tool: Hexagon head socket wrench no. 1.5.</td>
</tr>
</table>

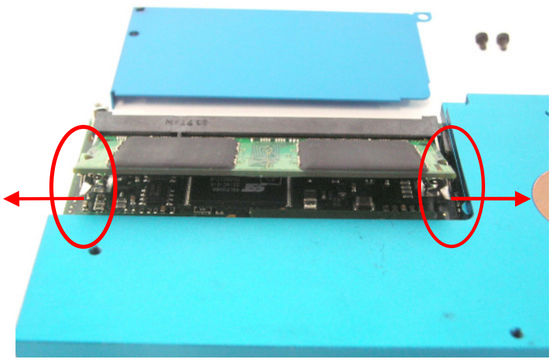


Step 3:

Remove the 2 screws from the SODIMM cover and dismantle the cover ***very carefully***. Slide the cover to the side and gently lift it away from the casing.

Screw Type: Cylinder hexagon socket type screw
M2x4mm / BN11 DIN912 ISO 4762

Tool: Hexagon head socket wrench no. 1.5



Step 4:

Using your thumbnails, gently push the clips holding the RAM module in place toward the outside. There will be a slight "click" and the RAM will flip up at an angle.

Remove the original RAM.

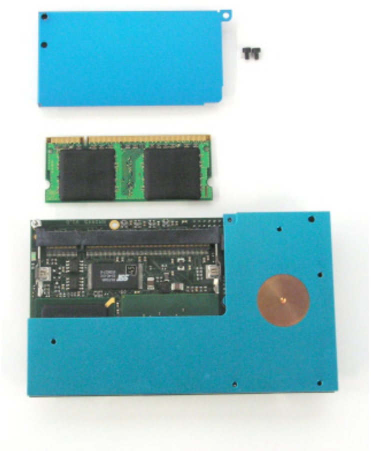
With the new RAM, carefully place the side with the connectors into the slot. There is only one correct way to place the RAM in the slot due to a notch between the connectors which matches up to a tab in the slot. Do ***not*** force the RAM into the slot, it should fit very easily.

Slowly push the RAM down until the clips "click" into place.

Step 5:

To reassemble the smartModule and heat sink, follow Steps 1-4 backwards.

In the case of an active heat sink, do not forget to connect it.



The photo shows the completely dismantled parts.

6.3. COMexpress Connector Description

6.3.1. Signal Terminology Descriptions

Signal	Description
PU	Internally implemented Pull up resistor
PD	Internally implemented Pull down resistor
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3.3VSB	Input 3.3V tolerant, active in standby state
O 3V	Output 3.3V signal level
O 5V	Output 5V signal level
P	Power Input/Output
D	Differential signal pair
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
SATA	In compliance with Serial ATA specification, Revision 1.0a
LVDS	Low Voltage Differential Signal-350mV nominal; 450mV maximum differential signal
LAN	100/10Mbit/s LAN signals coming from the PHY
TPM	Trusted Platform Module

6.3.2. COMexpress Connector Pinout

COMexpress type 2 (BUS on the smartModuleExpress 945) Connectors A / B: Pins 1-55

Pin	Group	Volt	Length	Signal	Pin	Group	Volt	Length	Signal
A1				GND	B1				GND
A2	LAN		D	MDI3-	B2	LAN	3.3V		LAN_ACTIVITY#
A3	LAN		D	MDI3+	B3	LPC	3.3V		LPC_FRAME#
A4	LAN	3.3V		SPEED100#	B4	LPC	3.3V		LPC_AD0
A5	LAN	3.3V		SPEED1000#	B5	LPC	3.3V		LPC_AD1
A6	LAN		D	MD2I-	B6	LPC	3.3V		LPC_AD2
A7	LAN		D	MD2+	B7	LPC	3.3V		LPC_AD3
A8	LAN	3.3V		LAN_LINK#	B8	LPC	3.3V		LPC_DRQ0#
A9	LAN		D	MDI1-	B9	LPC	3.3V		LPC_DRQ1#
A10	LAN		D	MDI1+	B10	LPC	3.3V		LPC_CLK
A11				GND	B11				GND
A12	LAN		D	MD0-	B12	PM	3.3V	Input	PWRBTN#
A13	LAN		D	MD0+	B13	SMB	3.3V		SMB_CLK
A14	LAN			CT-Ref	B14	SMB	3.3V		SMB_DAT
A15	PM	3.3V		SUS_S3#	B15	SMB	3.3V		SMB_ALERT#
A16	SATA0		D	SATA0-TX+	B16	SATA1		D	SATA1-TX+
A17	SATA0		D	SATA0-TX-	B17	SATA1		D	SATA1-TX-
A18	PM	3.3V		SUS_S4#	B18	PM	3.3V		SUS_STAT#
A19	SATA0		D	SATA0-RX+	B19	SATA1		D	SATA1-RX+
A20	SATA0		D	SATA0-RX0-	B20	SATA1		D	SATA1-RX-
A21				GND	B21				GND
A22	SATA2 **		D	NC	B22	SATA3 **		D	NC
A23	SATA2 **		D	NC	B23	SATA3 **		D	NC
A24	PM	3.3V		SUS_S5#	B24	PM	3.3V		PWR_OK
A25	SATA2 **		D	NC	B25	SATA3 **		D	NC
A26	SATA2 **		D	NC	B26	SATA3 **		D	NC
A27	PM	3.3V		BATLOW#	B27	PM	3.3V		WDT
A28	IDE	3.3V		ATA_ACTIVITY#	B28	AC97	3.3V		AC_SDIN2
A29	AC97	3.3V		AC_SYNCH	B29	AC97	3.3V		AC_SDIN1
A30	AC97	3.3V		AC_RST#	B30	AC97	3.3V		AC_SDIN0
A31				GND	B31				GND
A32	AC97	3.3V		AC_BITCLK	B32	Legacy	3.3V		Speaker Out
A33	AC97	3.3V		AC_SDOUT	B33	Not used	3.3V		I2C-CK
A34	BIOS	3.3V		BIOS_DISABLE#	B34	Not used	3.3V		I2C-DAT
A35	PM	3.3V		THRMTRIP#	B35	PM	3.3V		THRM#
A36	USB6		D	USB6-	B36	USB7		D	USB7-
A37	USB6		D	USB6+	B37	USB7		D	USB7+
A38	USB67OC	3.3V		USB_6_7_OC#	B38	USB45OC	3.3V		USB_4_5_OC#
A39	USB4		D	USB4-	B39	USB5		D	USB5-
A40	USB4		D	USB4+	B40	USB5		D	USB5+
A41				GND	B41				GND
A42	USB2		D	USB2-	B42	USB3		D	USB3-
A43	USB2		D	USB2+	B43	USB3		D	USB3+
A44	USB23OC	3.3V		USB_2_3_OC#	B44	USB01OC	3.3V		USB_0_1_OC#
A45	USB0		D	USB0-	B45	USB1		D	USB1-
A46	USB0		D	USB0+	B46	USB1		D	USB1+
A47	Supply			VCC_RTC	B47	PCIEX	3.3V		EXCD1_PERST#
A48	PCIEX	3.3V		EXCD0_PERST#	B48	PCIEX	3.3V		EXCD1_CPPE#
A49	PCIEX	3.3V		EXCD0_CPPE#	B49	Reset_In	3.3V		MAIN_IN_RESET#
A50	LPC	3.3V		LPC_SERIRQ	B50	Reset_Out	3.3V		CB_RESET# *
A51				GND	B51				GND
A52	PCIEX5		D	PCIe_TX5+	B52	PCIEX5		D	PCIe_RX5+
A53	PCIEX5		D	PCIe_TX5-	B53	PCIEX5		D	PCIe_RX5-
A54		3.3V		GPI 0	B54		3.3V		GPO 1
A55	PCIEX4		D	PCIe_TX4+	B55	PCIEX4		D	PCIe_RX4+

* The CB_Reset# is used to start the external Supply and works as Power_Enable.

** The SATA3/3 are not connected on the SMX945 because the 945GM has only 2 SATA ports!
Use only SATA0 and SATA1 with the SMX945 series Version 1.0.

COMexpress type 2 (Bus on smartModuleExpress 945) Connectors A / B: Pins 56-110

Pin	Group	Volt	Length	Signal	Pin	Group	Volt	Length	Signal
A56	PCIEX4		D	PCIe_TX4-	B56	PCIEX4		D	PCIe_RX4-
A57				GND	B57				GPO 2
A58	PCIEX3		D	PCIe_TX3+	B58	PCIEX3		D	PCIe_RX3+
A59	PCIEX3		D	PCIe_TX3-	B59	PCIEX3		D	PCIe_RX3-
A60				GND	B60				GND
A61	PCIEX2		D	PCIe_TX2+	B61	PCIEX2		D	PCIe_RX2+
A62	PCIEX2		D	PCIe_TX2-	B62	PCIEX2		D	PCIe_RX2-
A63				GPI 1	B63				GP0 3
A64	PCIEX1		D	PCIe_TX1+	B64	PCIEX1		D	PCIe_RX1+
A65	PCIEX1		D	PCIe_TX1-	B65	PCIEX1		D	PCIe_RX1-
A66				GND	B66	PM	3.3V		WAKE0#
A67		3.3V		GPI 2	B67	PM	3.3V		WAKE1#
A68	PCIEX0		D	PCIe_TX0+	B68	PCIEX0		D	PCIe_RX0+
A69	PCIEX0		D	PCIe_TX0-	B69	PCIEX0		D	PCIe_RX0-
A70				GND	B70				GND
A71	LVDS-A		D	LVDS_A0+	B71	LVDS-B		D	LVDS_B0+
A72	LVDS-A		D	LVDS_A0-	B72	LVDS-B		D	LVDS_B0-
A73	LVDS-A		D	LVDS_A1+	B73	LVDS-B		D	LVDS_B1+
A74	LVDS-A		D	LVDS_A1-	B74	LVDS-B		D	LVDS_B1-
A75	LVDS-A		D	LVDS_A2+	B75	LVDS-B		D	LVDS_B2+
A76	LVDS-A		D	LVDS_A2-	B76	LVDS-B		D	LVDS_B2-
A77	LVDS	3.3V		LVDS_VDD_EN	B77	Clock Out	3.3V		PCI_CLK4
A78	Clock Out	3.3V		48MHz	B78	Clock Out	3.3V		14MHz
A79	Clock Out	3.3V		CLKSIO_33MHz	B79	LVDS	3.3V		LVDS_BKLT_EN
A80				GND	B80				GND
A81	LVDS-A		D	LVDS_A_CLK+	B81	LVDS-B		D	LVDS_B_CLK+
A82	LVDS-A		D	LVDS_A_CLK-	B82	LVDS-B		D	LVDS_B_CLK-
A83	LVDS	3.3V		LVDS_I2C_CK	B83	LVDS	3.3V		LVDS_BKLT_CTRL
A84	LVDS	3.3V		LVDS_I2C_DAT	B84	POWER-In	5.0V		VCC5V_ALW In
A85				GPI 3	B85	POWER-In	5.0V		VCC5V_ALW In
A86	KB	3.3V		KBD_RST#	B86	POWER-In	5.0V		VCC5V_ALW In
A87	Legacy	3.3V		KBD_A20Gate	B87	POWER-In	5.0V		VCC5V_ALW In
A88	PCIEX0		D	PCIe0_CK_REF+	B88	Power Out	5.0V	*	VCC5 output
A89	PCIEX0		D	PCIe0_CK_REF-	B89	VGA	A		VGA-RED
A90				GND	B90				GND
A91	Power Out		*	VCC3.3V Out	B91	VGA	A		VGA – GREEN
A92	Power Out		*	VCC3.3V Out	B92	VGA	A		VGA – BLUE
A93		3.3V		GPO 0	B93	VGA	5.0V		VGA - HSYNCH
A94	Power Out		*	3.3V Alw Out	B94	VGA	5.0V		VGA - VSYNCH
A95	Power Out		*	3.3V Alw Out	B95	VGA	3.3V		VGA_I2C_CLK
A96				GND	B96	VGA	3.3V		VGA_I2C_DAT
A97	Power-In			+12Volt	B97	TV-Out	A		TV_DAC_A
A98	Power-In			+12Volt	B98	TV-Out	A		TV_DAC_B
A99	Power-In			+12Volt	B99	TV-Out	A		TV_DAC_C
A100				GND	B100				GND
A101	Power-In			+12Volt	B101	Power-In			+12Volt Input
A102	Power-In			+12Volt	B102	Power-In			+12Volt Input
A103	Power-In			+12Volt	B103	Power-In			+12Volt Input
A104	Power-In			+12Volt	B104	Power-In			+12Volt Input
A105	Power-In			+12Volt	B105	Power-In			+12Volt Input
A106	Power-In			+12Volt	B106	Power-In			+12Volt Input
A107	Power-In			+12Volt	B107	Power-In			+12Volt Input
A108	Power-In			+12Volt	B108	Power-In			+12Volt Input
A109	Power-In			+12Volt	B109	Power-In			+12Volt Input
A110				GND	B110				GND

* These voltages are generated in the smartModule and are only connected for monitoring.
Do not supply external circuits with these voltages.

COMexpress type 2 (BUS on the smartModuleExpress 945) Connectors C / D: Pins 1-55

Pin	Group	Volt	Length	Signal	Pin	Group	Volt	Length	Signal
C1				GND	D1				GND
C2	IDE	3.3V		IDE-D7	D2	IDE	3.3V		IDE-D5
C3	IDE	3.3V		IDE-D6	D3	IDE	3.3V		IDE-D10
C4	IDE	3.3V		IDE-D3	D4	IDE	3.3V		IDE-D11
C5	IDE	3.3V		IDE-D15	D5	IDE	3.3V		IDE-D12
C6	IDE	3.3V		IDE-D8	D6	IDE	3.3V		IDE-D4
C7	IDE	3.3V		IDE-D9	D7	IDE	3.3V		IDE-D0
C8	IDE	3.3V		IDE-D2	D8	IDE	3.3V		IDE-REQ
C9	IDE	3.3V		IDE-D13	D9	IDE	3.3V		IDE-IOW#
C10	IDE	3.3V		IDE-D1	D10	IDE	3.3V		IDE-ACK
C11				GND	D11				GND
C12	IDE	3.3V		IDE-D14	D12	IDE	3.3V		IDE-IRQ
C13	IDE	3.3V		IDE-IORDY	D13	IDE	3.3V		IDE-A0
C14	IDE	3.3V		IDE-IOR#	D14	IDE	3.3V		IDE-A1
C15	PCI	3.3V		PCI_PME#	D15	IDE	3.3V		IDE_A2
C16	PCI	3.3V		PCI_GNT2#	D16	IDE	3.3V		IDE_CS1#
C17	PCI	3.3V		PCI_REQ2#	D17	IDE	3.3V		IDE_CS3#
C18	PCI	3.3V		PCI_GNT1#	D18	IDE	3.3V		IDE_RESET#
C19	PCI	3.3V		PCI_REQ1#	D19	PCI	3.3V		PCI_GNT3#
C20	PCI	3.3V		PCI_GNT0#	D20	PCI	3.3V		PCI_REQ3#
C21				GND	D21				GND
C22	PCI	3.3V		PCI_REQ0#	D22	PCI	3.3V		PCI_AD1
C23	PCI *	3.3V	Out	PCI_RESET#_Out	D23	PCI	3.3V		PCI_AD3
C24	PCI	3.3V		PCI_AD0	D24	PCI	3.3V		PCI_AD5
C25	PCI	3.3V		PCI_AD2	D25	PCI	3.3V		PCI_AD7
C26	PCI	3.3V		PCI_AD4	D26	PCI	3.3V		PCI_C/BE0#
C27	PCI	3.3V		PCI_AD6	D27	PCI	3.3V		PCI_AD9
C28	PCI	3.3V		PCI_AD8	D28	PCI	3.3V		PCI_AD11
C29	PCI	3.3V		PCI_AD10	D29	PCI	3.3V		PCI_AD13
C30	PCI	3.3V		PCI_AD12	D30	PCI	3.3V		PCI_AD15
C31				GND	D31				GND
C32	PCI	3.3V		PCI_AD14	D32	PCI	3.3V		PCI_PAR
C33	PCI	3.3V		PCI_C/BE1#	D33	PCI	3.3V		PCI_SERR#
C34	PCI	3.3V		PCI_PERR#	D34	PCI	3.3V		PCI_STOP#
C35	PCI	3.3V		PCI_LOCK#	D35	PCI	3.3V		PCI_TRDY#
C36	PCI	3.3V		PCI_DEVSEL#	D36	PCI	3.3V		PCI_FRAME#
C37	PCI	3.3V		PCI_IRDY#	D37	PCI	3.3V		PCI_AD16
C38	PCI	3.3V		PCI_C/BE2#	D38	PCI	3.3V		PCI_AD18
C39	PCI	3.3V		PCI_AD17	D39	PCI	3.3V		PCI_AD20
C40	PCI	3.3V		PCI_AD19	D40	PCI	3.3V		PCI_AD22
C41				GND	D41				GND
C42	PCI	3.3V		PCI_AD21	D42	PCI	3.3V		PCI_AD24
C43	PCI	3.3V		PCI_AD23	D43	PCI	3.3V		PCI_AD26
C44	PCI	3.3V		PCI_C/BE3#	D44	PCI	3.3V		PCI_AD28
C45	PCI	3.3V		PCI_AD25	D45	PCI	3.3V		PCI_AD30
C46	PCI	3.3V		PCI_AD27	D46	PCI	3.3V		PCI_IRQC#
C47	PCI	3.3V		PCI_AD29	D47	PCI	3.3V		PCI_IRQD#
C48	PCI	3.3V		PCI_AD31	D48	PCI	3.3V		PCI_CLKRUN#
C49	PCI	3.3V		PCI_IRQA#	D49	PCI	3.3V		PCI_M66EN
C50	PCI	3.3V		PCI_IRQB#	D50	PCI	3.3V		PCI_CLK
C51				GND	D51				GND
C52	PEG		D	PEG_RX0+	D52	PEG		D	PEG_TX0+
C53	PEG		D	PEG_RX0-	D53	PEG		D	PEG_TX0-
C54	BIOS / Type-In	OC		FWH_TBL / TYPE0	D54	PEG			PEG_LANE_RV#
C55	PEG		D	PEG_RX1+	D55	PEG		D	PEG_TX1+

* PCI_Reset# [C23] is used as a reset for all LPC, PCI and PCIexpress devices. Use a 74HC08 supplied with 3.3V as a buffer to generate different reset groups (Reset_PCI#, Reset_PCIex#, Reset_LPC# , etc.).

COMexpress type 2 (Bus on smartModuleExpress 945) Connectors C / D: Pins 56-110

Pin	Group	Volt	Length	Signal	Pin	Group	Volt	Length	Signal
C56	PEG		D	PEG_RX1-	D56	PEG		D	PEG_TX1-
C57	Type-In	OC		TYPE1#	D57	PCI	3.3V		GNT4#
C58	PEG		D	PEG_RX2+	D58	PEG		D	PEG_TX2+
C59	PEG		D	PEG_RX2-	D59	PEG		D	PEG_TX2-
C60				GND	D60				GND
C61	PEG		D	PEG_RX3+	D61	PEG		D	PEG_TX3+
C62	PEG		D	PEG_RX3-	D62	PEG		D	PEG_TX3-
C63	PCI			P-IRQ-E#	D63	PCI			P-IRQ-G#
C64	PCI			P-IRQ-F#	D64	PCI			P-IRQ-H#
C65	PEG		D	PEG_RX4+	D65	PEG		D	PEG_TX4+
C66	PEG		D	PEG_RX4-	D66	PEG		D	PEG_TX4-
C67				Reserved / NC	D67				GND
C68	PEG		D	PEG_RX5+	D68	PEG		D	PEG_TX5+
C69	PEG		D	PEG_RX5-	D69	PEG		D	PEG_TX5-
C70				GND	D70				GND
C71	PEG		D	PEG_RX6+	D71	PEG		D	PEG_TX6+
C72	PEG		D	PEG_RX6-	D72	PEG		D	PEG_TX6-
C73	SDVO			SDVO_DATA	D73	SDVO			SDVO_CLK
C74	PEG		D	PEG_RX7+	D74	PEG		D	PEG_TX7+
C75	PEG		D	PEG_RX7-	D75	PEG		D	PEG_TX7-
C76				GND	D76				GND
C77	PCI	3.3V		REQ4#	D77	IDE	3.3V		PATA_Detect#
C78	PEG		D	PEG_RX8+	D78	PEG		D	PEG_TX8+
C79	PEG		D	PEG_RX8-	D79	PEG		D	PEG_TX8-
C80				GND	D80				GND
C81	PEG		D	PEG_RX9+	D81	PEG		D	PEG_TX9+
C82	PEG		D	PEG_RX9-	D82	PEG		D	PEG_TX9-
C83				REQ5#	D83				GNT5#
C84				GND	D84				GND
C85	PEG		D	PEG_RX10+	D85	PEG		D	PEG_TX10+
C86	PEG		D	PEG_RX10-	D86	PEG		D	PEG_TX10-
C87				GND	D87				GND
C88	PEG		D	PEG_RX11+	D88	PEG		D	PEG_TX11+
C89	PEG		D	PEG_RX11-	D89	PEG		D	PEG_TX11-
C90				GND	D90				GND
C91	PEG		D	PEG_RX12+	D91	PEG		D	PEG_TX12+
C92	PEG		D	PEG_RX12-	D92	PEG		D	PEG_TX12-
C93				GND	D93				GND
C94	PEG		D	PEG_RX13+	D94	PEG		D	PEG_TX13+
C95	PEG		D	PEG_RX13-	D95	PEG		D	PEG_TX13-
C96				GND	D96				GND
C97	BIOS	3.3V		FWH_INIT#	D97	PEG	3.3V		PEG_ENABLE#
C98	PEG		D	PEG_RX14+	D98	PEG		D	PEG_TX14+
C99	PEG		D	PEG_RX14-	D99	PEG		D	PEG_TX14-
C100				GND	D100				GND
C101	PEG		D	PEG_RX15+	D101	PEG		D	PEG_TX15+
C102	PEG		D	PEG_RX15-	D102	PEG		D	PEG_TX15-
C103				GND	D103				GND
C104	Power In	12V		+12Volt	D104	Power In	12V		+12Volt
C105	Power In	12V		+12Volt	D105	Power In	12V		+12Volt
C106	Power In	12V		+12Volt	D106	Power In	12V		+12Volt
C107	Power In	12V		+12Volt	D107	Power In	12V		+12Volt
C108	Power In	12V		+12Volt	D108	Power In	12V		+12Volt
C109	Power In	12V		+12Volt	D109	Power In	12V		+12Volt
C110				GND	D110				GND

6.3.3. COMexpress Connector Specifications

The Kontron Compact Computers smartModuleX945 module connectors are surface-mounted, 0.5mm pitch, 220pin connectors.

Parameter	Condition:	Specification
Material	Contact:	Copper Alloy
	Housing:	Thermoplastic Molded Compound L.C.P
Electrical	Current:	0.5 Amp
	Voltage:	50 VAC
	Termination Resistance:	55mΩ max. ΔR = 20mΩ max.
	Insulation Resistance:	500MΩ
Mechanical	Mating Cycles:	30
	Connector Mating Force:	0.9N per contact
	Connector Unmating Force:	0.1N per contact
	Pitch:	0.5mm
	Number of pins:	220
	Temperature rating:	-40°C to 85°C

The manufacturer of the connector is:

Source on smartBusX945 module *	Part Name	Part Number
Carrier Board Connector		
TYCO / AMP	H = 8mm Standard H = 5mm Alternative	8-6318491-6 3-1827253-6
SMX945/915 COMexpress Connector		
TYCO / AMP	Mating connector	8-1318490-6

The stack height may be defined on the carrier board as either 5 or 8mm using the two different connector types available.

6.3.4. SDVO / PEG Multiplexed Signals

The Kontron Compact Computers (KCC) smartModuleX945 uses the upper PEG signals to multiplex the two SDVO channels. If the SDVO is in use, the PEG function is not available. Intel allows, with the P45CM, multiplexing the SDVO on the lower or, alternatively, on the upper PEG lines. KCC's implementation for multiplexing the upper PEG lines are defined in the table below.

Pin	PEG Function	SDVO Function
D78	PEG_TX8+	SDVO_Channel_C_CLK+
D79	PEG_TX8-	SDVO_Channel_C_CLK-
D81	PEG_TX9+	SDVO_Channel_C_Blue+
D82	PEG_TX9-	SDVO_Channel_C_Blue-
D85	PEG_TX10+	SDVO_Channel_C_Green+
D86	PEG_TX10-	SDVO_Channel_C_Green-
D88	PEG_TX11+	SDVO_Channel_C_Red+
D89	PEG_TX11-	SDVO_Channel_C_Red-
C85	PEG_RX10+	SDVO_Channel_C_INT+
C86	PEG_RX10-	SDVO_Channel_C_INT-
D91	PEG_TX12+	SDVO_Channel_B_CLK+
D92	PEG_TX12-	SDVO_Channel_B_CLK-
D94	PEG_TX13+	SDVO_Channel_B_Blue+
D95	PEG_TX13-	SDVO_Channel_B_Blue-
D98	PEG_TX14+	SDVO_Channel_B_Green+
D99	PEG_TX14-	SDVO_Channel_B_Green-
D101	PEG_TX15+	SDVO_Channel_B_Red+
D102	PEG_TX15-	SDVO_Channel_B_Red-
C98	PEG_RX14+	SDVO_Channel_B_INT+
C99	PEG_RX14-	SDVO_Channel_B_INT-
C101	PEG_TX15+	SDVO_TVCLK_Input+
C102	PEG_TX15-	SDVO_TVCLK_Input-
C94	PEG_RX13+	SDVO_STALL+
C95	PEG_RX13-	SDVO_STALL-
D97 PEG-Enable	0Volt	Open
C73	Not used	SDVO_DATA
D73	Not used	SDVO_CLK
Buffered with (74HC08) from the PCI-Reset# Pin C23	PEG_RESET	SDVO_Reset

6.4. Signal Loss

COM Express™ module and carrier board insertion-loss budgets for the PCI Express, SATA, USB and GBE interfaces are presented in the following sections.

These budgets were formulated to be compatible with the relevant source specifications. The source specifications vary in their treatment of insertion-loss parameters. For example, the PCI Express Card Electromechanical Specification factors cross-talk losses into the insertion-loss budgets, but the SATA, USB and GBE source specifications do not.

There is no explicit COM Express™ jitter budget for the high speed differential interfaces. Designers should refer to the relevant source specifications (PCIE, SATA, USB and GBE) for system jitter budgets.

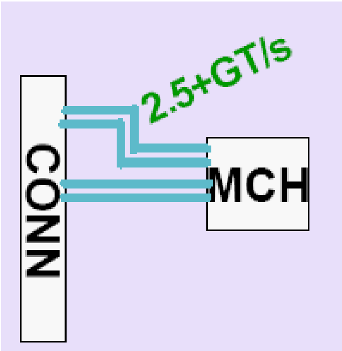
For frequency-dependent material losses, a rule-of-thumb insertion-loss value of 0.28 dB per inch per GHz is used in all cases, representative of commonly used FR4 PCB laminates. This value is consistent with the PCI Express Card Electromechanical Specification usage (which calls out a 1.4 dB material loss for 4 inches of trace at 1.25 GHz). It is also consistent with other PICMG® specifications that use values slightly above and below this value.

Module and carrier board vendors may elect to use PCB laminates with better characteristics than common FR4. If this is done, then the trace lengths referenced in the following sections may be extended as long as the net insertion-loss budgets are met.

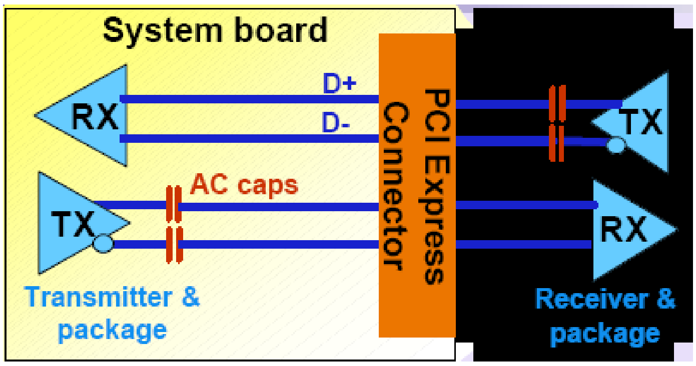
Loss budgets for future generations of PCI Express (Gen 2), Ethernet (10 Gb/s) and SATA (Gen 3) will be addressed in future revisions to this document.

6.5. Layout of High Speed Signals:

6.5.1. Design Rules for PCIexpress

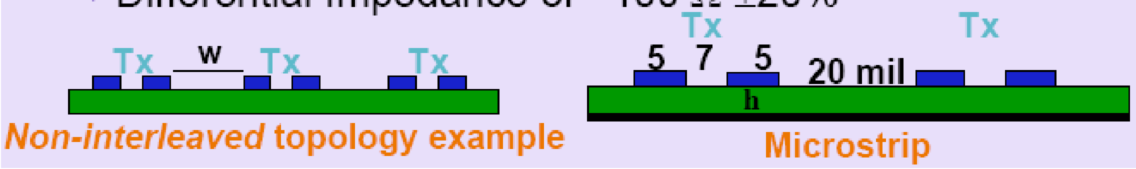


Point-to-point, match per data pair only

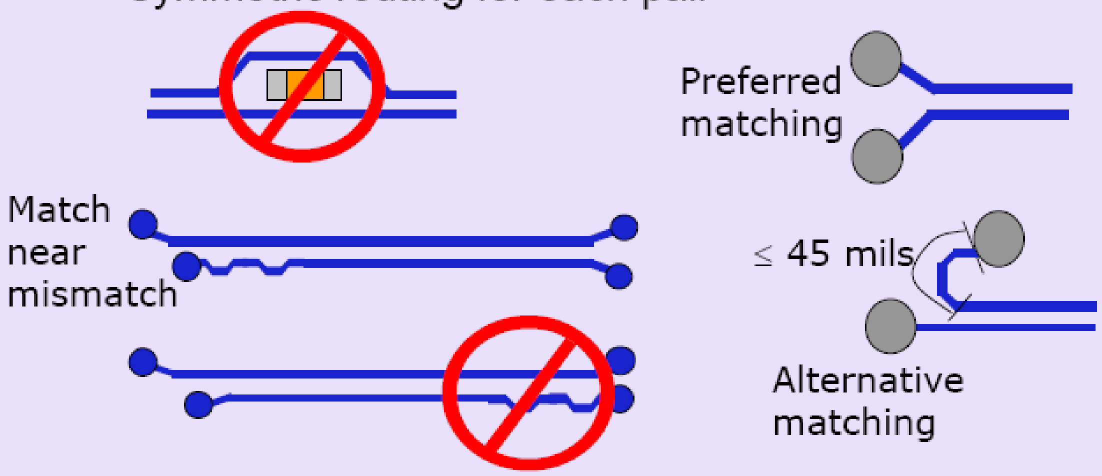


TX must be AC coupled
up to 12" long, 0.3dB loss per inch
max. 13.2 dB loss and 300ps jitter between TX - RX!

- Example impedance targets:
  - ✓Single-end Z_0 of 60 Ω ±15%
  - ✓Differential Impedance of ~100 Ω ±20%

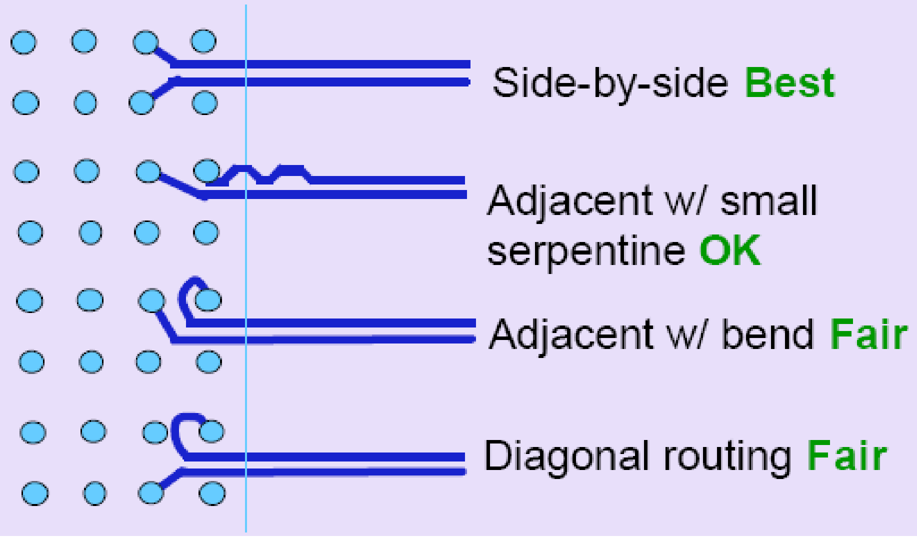


- No matching needed pair-to-pair
- Match each differential pair per segment
  - ✓Match overall length ≤ 5 mils (recommended)
  - ✓Symmetric routing for each pair

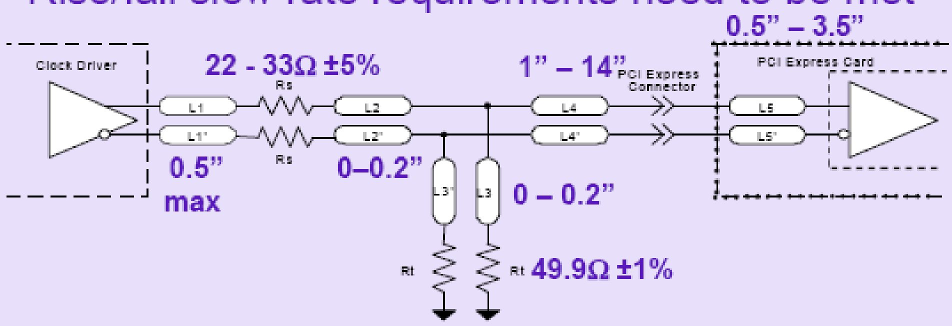


6.5.2. Layout Rules

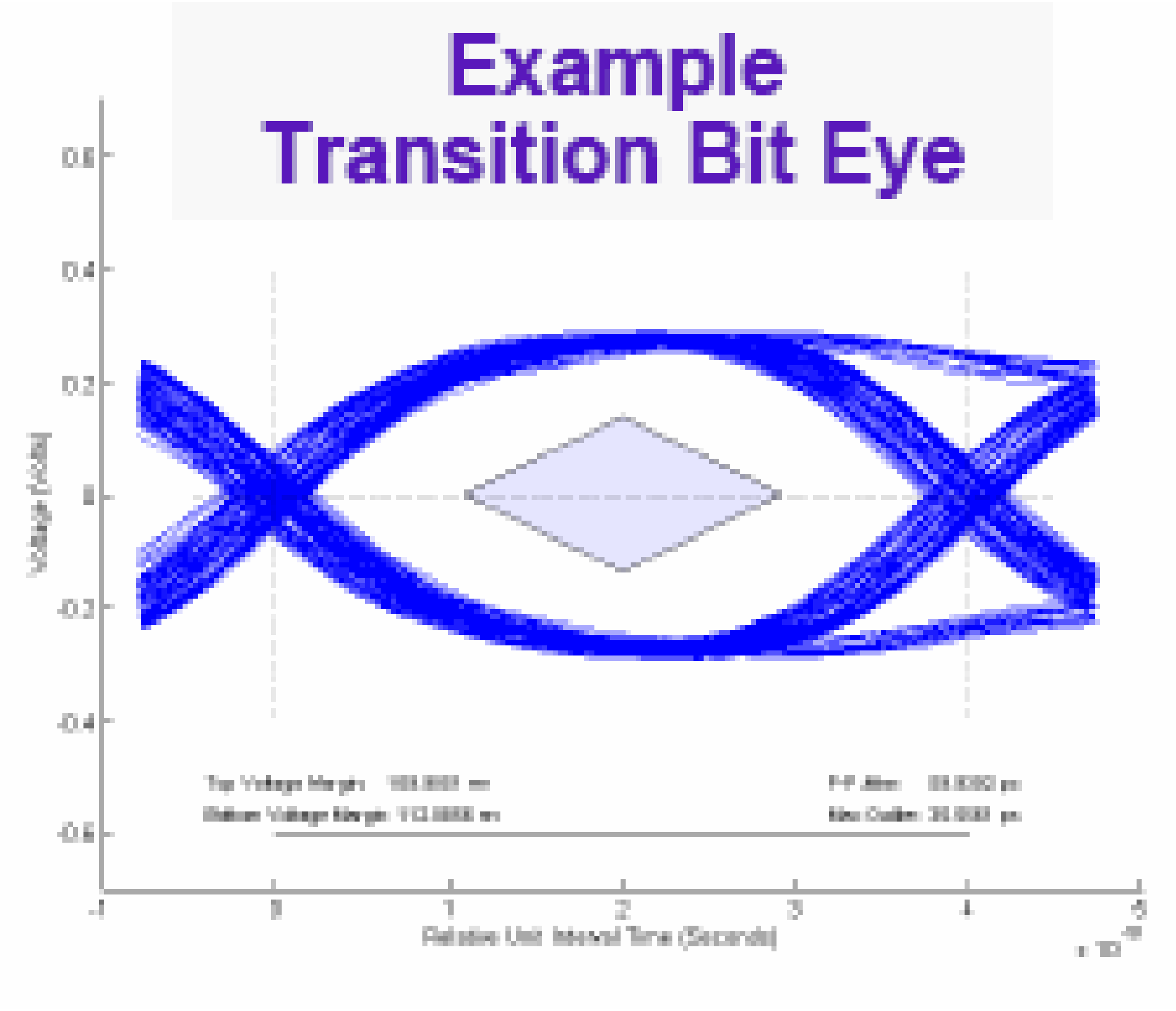
- Use side-by-side breakout for package to maintain symmetry
- Avoid tight bends



- Clocks have no phase relationships
  - ✓Length matching for clocks is *NOT* required!
- Deliver diff clock to each device and connector
  - ✓Use same trace geometries as other diff pairs
- *Clock driver requirements:*
  - ✓100MHz with SSC support (e.g. CK410)
  - ✓System board (source) termination only
  - ✓Rise/fall slew rate requirements need to be met



6.5.3. Eye Diagram with 6GHz/20GS Digital Scope



6.6. Signal Descriptions

Signal	Description	I/O	Termination	Remarks
VCC	Power Supply +5VDC ±5%	P		External supply for external peripheral
GND	Power Ground	P		External supply
3.3V	Power Supply +3.3VDC	P		External supply for external peripheral
NC	Not Connected	N.A.		Do not connect
SERIRQ	Serial Interrupt request	I 3.3V	PU 10K 3.3V	
PCICLK1-4	Clock output	O 3.3V		
REQ0-3#	Bus request	I 3.3V	PU 8k2 3.3V	REQ1-3# is a boot strap signal, 5V Tolerant
GNT0-3#	Bus grant	O 3.3V		GNT2/3# is a boot strap signal
AD0-31	Address/Data bus lines	I/O 3.3V		5V Tolerant
CBE0-3#	Bus command/byte enables	I/O 3.3V		5V Tolerant
PAR	Bus parity	I/O 3.3V		5V Tolerant
SERR#	Bus system error	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PERR#	Bus grant parity error	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PME#	Bus power management event	I/O 3.3VSB	PU 8k2 3.3V SB	
LOCK#	Bus lock	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
DEVSEL#	Bus device select	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
TRDY#	Bus target ready	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
IRDY#	Bus initiator ready	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
STOP#	Bus stop	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
FRAME#	Bus frame	I/O 3.3V	PU 8k2 3.3V	5V Tolerant
PCIRST#	Bus reset	O 3.3V		Asserted during system reset
INTA#	Bus interrupt A	I 3.3V	PU 8k2 3.3V	5V Tolerant
INTB#	Bus interrupt B	I 3.3V	PU 8k2 3.3V	5V Tolerant
INTC#	Bus interrupt C	I 3.3V	PU 8k2 3.3V	5V Tolerant
INTD#	Bus interrupt D	I 3.3V	PU 8k2 3.3V	5V Tolerant
PCI_Reset#	Bus Reset#	O 3.3V		Generated out of Pin C23 with a 74HC08 buffer (3.3V)

COM Express™ specifies only a single copy of the PCI clock for off-module use. If only one carrier board PCI device is implemented, then that single clock may be routed to the device. If more than one carrier board PCI device is implemented, then the carrier board should replicate the PCI clock using a zero delay buffer. COM Express™ carrier board implementations should allow 1.6 ns +/- 0.1 ns for the PCI clock propagation delay from the COM Express™ module connector pin to the destination device pin.

Propagation delay varies with construction details such as trace geometry, PCB stack up, and PCB material dielectric constant. Propagation delay values of 140ps/inch to 180ps/inch are common for outer layer traces. A propagation delay value of 180ps/inch is common for inner layer traces/carrier boards.

Using 180ps/inch as the propagation delay value for an inner layer carrier board PCI clock, then the COM Express™ carrier board delay of 1.6 ns works out to 8.88 inches of trace. If the destination device is on an add-on card, then the propagation delay associated with the 2.5 inches of add-on card trace are deducted from the 1.6 ns. Using 160ps/inch as a typical value for an outer layer slot card clock trace, the 2.5 inches of slot card clock trace length work out to a propagation delay of 0.4 ns. The carrier board PCI clock delay in this example would be 1.6 ns - 0.4 ns or 1.2 ns.

The PCI Local Bus Specification requires that:

- PCI clocks be synchronous within a 2 ns window at the destination devices
- the maximum propagation delay for the clock be 10 ns
- PCI slot-based add-on cards implement a PCI clock trace length of 2.5 inches

T_{MD} Propagation delay: module PCI clock source to on-module PCI device

T_{MC} Propagation delay: module PCI clock source to module connector PCI clock pin

T_{CD} Propagation delay: module connector to carrier board device

Fixed by COM Express™ Specification at 1.6 ns

T_{CS} Propagation delay: module connector to slot connector pin

P_{SD} Inverse propagation speed: slot card connector pin to slot card device

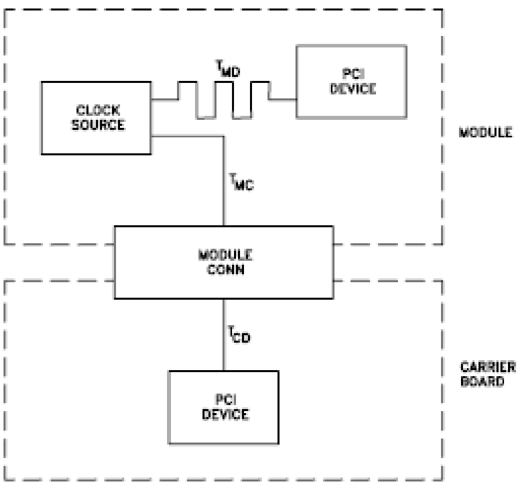
$T_{MD} = T_{MC} + T_{CD}$

$T_{MD} = T_{MC} + T_{CS} + L_{SD} * P_{SD}$

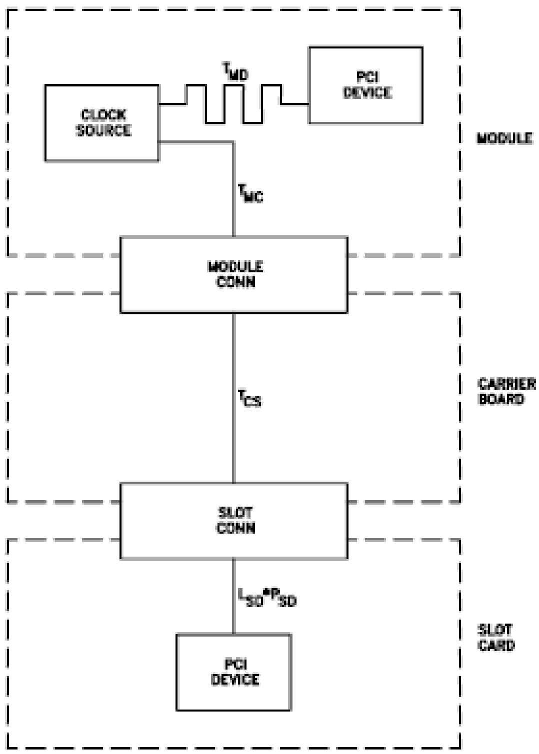
$T_{CS} = T_{CD} – L_{SD}*P_{SD}$

The parameters T_{MD} and T_{MC} apply to module designs. Module designers ***should*** minimize T_{MC}, and then arrange that T_{MD} satisfies the relation $T_{MD} = T_{MC} + T_{CD}$.

Carrier board located PCI device



Slot board located PCI device



LSD Length: slot card connector pin to slot card device. The following definitions and equations apply:
Fixed by PCI Local Bus Specification at 2.5 inches (units of time/length)
Determined by slot card PCB design; typical value is 160ps/inch.

Signal	Description	I/O	Termination	Remarks
USB0	USB Port 0, data + or D+	I/O 3.3V		USB 2.0 compliant
USB0#	USB Port 0, data - or D-	I/O 3.3V		USB 2.0 compliant
to				
USB7	USB Port 7, data + or D+	I/O 3.3V		USB 2.0 compliant
USB7	USB Port 7, data - or D-	I/O 3.3V		USB 2.0 compliant

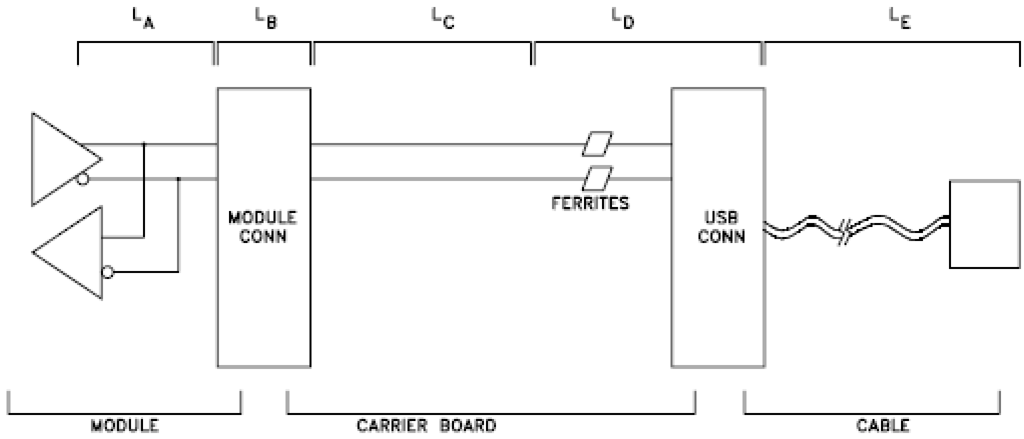


Table 5-19: USB Insertion Loss Budget, 400 MHz

Segment	Loss (dB)	Notes
L_A	0.67	Up to 6 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.05	COM Express™ connector at 400 MHz measured value
L_C	1.68	Up to 14 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	1.00	USB connector and ferrite loss
L_E	5.80	USB cable and far end connector loss, per source specification
Total	9.20	

Signal	Description	I/O	Termination	Remarks
LPC_AD[0-3]	Multiplexed Command, Address and Data	I/O 3.3V		
LPC_FRAME#	Frame: Indicates the start of a new cycle or termination of a broken cycle	O 3.3V		
LPC_DRQ[0-1]#	Encoded DMA/Bus Master Request. I 3.3V	I 3.3V	PU 10k 3.3V	
LPC_Reset#	Reset#	O 3.3V		Generated from the PCI_Reset# Signal.

Carrier Board LPC devices ***should*** be clocked with the LPC clock provided by the module interface. LPC clock length guidelines are the same as those for the PCI clock.

Carrier Board LPC devices ***should*** be reset with signal CB_RESET#.

Signal	Description	I/O	Termination	Remarks
SATA0_RX+	Serial ATA channel 0	I SATA		SATA-Spec. 1.0a
SATA0_RX-	Receive Input differential pair			
SATA0_TX+	Serial ATA channel 0	O SATA		SATA-Spec. 1.0a
SATA0_TX-	Transmitter Output differential pair			
SATA1_RX+	Serial ATA channel 1	I SATA		SATA-Spec. 1.0a
SATA1_RX-	Receive Input differential pair			
SATA1_TX+	Serial ATA channel 1	O SATA		SATA-Spec. 1.0a
SATA1_TX-	Transmitter Output differential pair			

The COM Express™ SATA insertion-loss budgets, presented below, represent the material losses and do not include cross-talk losses. The COM Express™ SATA insertion-loss budgets are a guideline: module and carrier board vendors ***should not*** exceed the values shown in the tables below.

The Serial ATA source specification provides insertion-loss figures only for the SATA cable. There are several cable types defined with insertion-losses ranging from 6 dB up to 16 dB. Cross-talk losses are separate from material losses in the SATA specification.

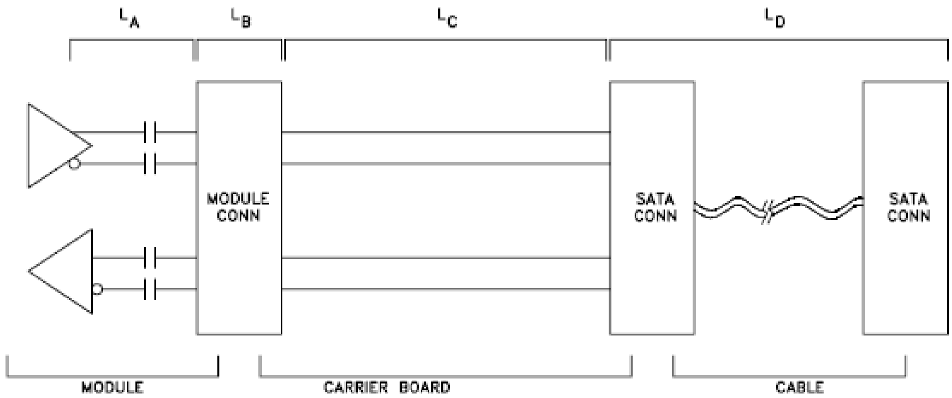


Table 5-17: SATA Gen 1 Insertion Loss Budget, 1.5 GHz

Segment	Loss (dB)	Notes
L_A	1.26	Up to 3.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.25	COM Express™ connector at 1.5 GHz measured value
L_C	3.07	Up to 7.2 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

Table 5-18: SATA Gen 2 Insertion Loss Budget, 3.0 GHz

Segment	Loss (dB)	Notes
L_A	1.68	Up to 2.0 inches of module trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40	
L_B	0.38	COM Express™ connector at 3.0 GHz measured value
L_C	2.52	Up to 3.0 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	6.00	Source specification cable and cable connector allowance
Total	10.98	

Signal	Description	I/O	Termination	Remarks
PCIE0_RX+	PCI Express channel 0			
PCIE0_RX-	Receive Input differential pair	I PCIE		Spec. 1.0A
PCIE0_TX+	PCI Express channel 0			
PCIE0_TX-	Transmit Output differential pair	O PCIE		Spec. 1.0A
PCIE1_RX+	PCI Express channel 1			
PCIE1_RX-	Receive Input differential pair	I PCIE		Spec. 1.0A
PCIE1_TX+	PCI Express channel 1			
PCIE1_TX-	Transmit Output differential pair	O PCIE		Spec. 1.0A
PCIE2_RX+	PCI Express channel 2			
PCIE2_RX-	Receive Input differential pair	I PCIE		Spec. 1.0A
PCIE2_TX+	PCI Express channel 2			
PCIE2_TX-	Transmit Output differential pair	O PCIE		Spec. 1.0A
PCIE3_RX+	PCI Express channel 3			
PCIE3_RX-	Receive Input differential pair	I PCIE		Spec. 1.0A
PCIE3_TX+	PCI Express channel 3			
PCIE3_TX-	Transmit Output differential pair	O PCIE		Spec. 1.0A
PCIE_CLK_REF+	PCI Express Reference Clock	0 PCIE	PD 50Ohm	Spec 1.0a
PCIE_CLK_REF-	or Lanes 0 to 3			
PCE_WAKE#	PCI Express Wake Event	I 3.3VSB	PU 1K 3.3VSB	Sideband wake signal asserted by components requesting wakeup
PCIE_Reset#	Reset#	O 3.3V		Generated from the PCI_Reset#, coming from Pin C23, buffered with a 74HC08 (3.3V).

The insertion losses previously allowed for the slot card and slot card connector are re-allocated for use on the carrier board, allowing longer carrier board trace lengths and more carrier board design flexibility. The module and COM Express™ connector-loss budgets remain the same.

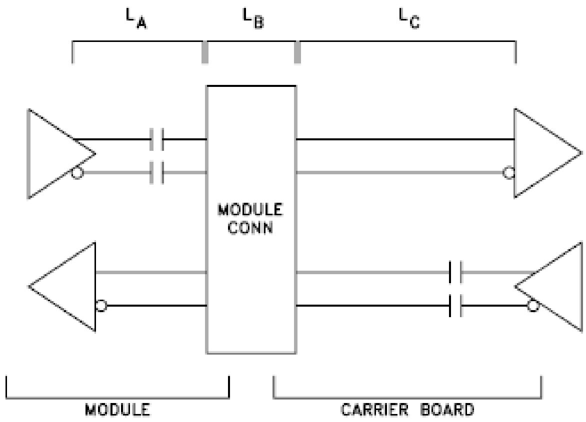


Table 5-16: PCI Express Insertion Loss Budget, 1.25 GHz with Carrier Board PCIE Device

Segment	Loss (dB)	Notes
L_A	3.46	Allowance for 5.15 inches of module trace @ 0.28 dB / GHz / inch and 1.66 dB crosstalk allowance. Coupling caps not included.
Coupling Caps	1.19	From PCI Express Card Electromechanical Spec., Rev. 1.1, parameters (L_{ST} – L_{SR}). Includes crosstalk allowance of 0.79 dB.
L_B	0.25	COM Express™ connector at 1.25 GHz measured value.
L_C	8.30	Allowance for 15.85 inches of Carrier Board trace @ 0.28 dB / GHz / inch and a 2.75 dB crosstalk allowance.
Total	13.20	

The module's transmit and receive insertion-loss budgets are different due to the presence of the coupling caps in the module transmit path. The module transmit path insertion-loss budget shall be 4.65 dB (3.46 dB + 1.19 dB). The module receive-path insertion-loss budget shall be 3.46 dB. COM Express™ connector loss is accounted for separately.

The carrier board's transmit and receive insertion-loss budgets are different due to the presence of the coupling caps in the carrier board transmit path. The carrier board transmit path insertion-loss budget shall be 9.49 dB (8.30 dB + 1.19 dB). The carrier board receive path insertion-loss shall be 8.30 dB. COM Express™ connector loss is accounted for separately.

Signal	Description	I/O	Termination	Remarks
AC_RST#	CODEC Reset	O 3.3V		
AC_SYN	Serial Bus Synchronization	O 3.3V		AC_SYNC is a boot strap AC_SYNC is a boot strap
AC_BIT_CLK	12.228MHz Serial Bit Clock from CODEC	O 3.3V		
AC_SDOUT	Audio Serial Data Output to CODEC	O 3.3V		AC_SDOUT is a boot strap signal (see note below)
AC_SDIN[0-2]	Audio Serial Data Input from CODEC0-CODEC2	I 3.3V		Only AC_SDIN2 is PD 10k

Note...
Not available: CODECDISABLE Disable onboard Audio Codec I 3.3V PD 10k

Signal	Description	I/O	Termination	Remarks
MD0+	LAN channel 0			
MD0-	Differential pair	D		Intel LAN PHY
MD1+	LAN channel 1			
MD1-	Differential pair	D		Intel LAN PHY
MD2+	LAN channel 2			
MD2-	Differential pair	D		Intel LAN PHY
MD3+	LAN channel 3			
MD3-	Differential pair	D		Intel LAN PHY
ACTLED#	Ethernet activity LED	O 3.3V		
LILED#	Ethernet link LED	O 3.3V		
SPEEDLED#	Ethernet speed LED, (ON at 100M)	O 3.3V		

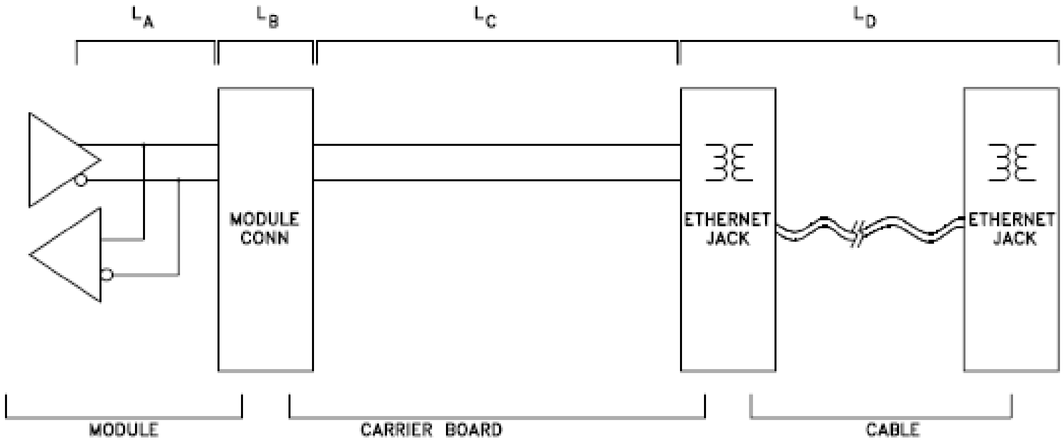


Table 5-20: 10/100/1000 Ethernet Insertion Loss Budget, 100 MHz

Segment	Loss (dB)	Notes
L_A	0.08	Up to 3 inches of module trace @ 0.28 dB / GHz / inch
L_B	0.02	COM Express™ connector at 100 MHz measured value
L_C	0.15	Up to 5 inches of Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00	Cable and cable connectors, integrated magnetics, per source spec.
Total	24.25	

Signal	Description	I/O	Termination	Remarks
HSYNCH	Horizontal Synchronization Pulse	O 3.3V		
VSYNCH	Vertical Synchronization Pulse	O 3.3V		
R	Red-channel RGB Analog Video	O	PD 150R	Analog output
G	Green-channel RGB Analog Video	O	PD 150R	Analog output
B	Blue-channel RGB Analog Video	O	PD 150R	Analog output
DDCK	Display Data Channel Clock	I/O 5V	PU 2k2 5V	
DDDA	Display Data Channel Data	I/O 5V	PU 2k2 5V	

Signal	Description	I/O	Termination	Remarks
SYNC	Composite sync	NC		Not supported
Y	Luminance for S-Video or Red for SCART	O	PD 150R	Analog output
C	Chrominance for S-Video or Green for SCART	O	PD 150R	Analog output
COMP	Composite Video or Blue for SCART	O	PD 150R	Analog output

Signal	Description	I/O	Termination	Remarks
DIGON	Controls display Power ON	O 5V	PD 10k	
BLON#	Controls display Backlight ON	O 5V		
LCDDO0-19	LVDS channel data 0-19	O LVDS		
DETECT#	Panel hot-plug detection	NC		Not supported
FPDDC_CLK	DDC lines used for flat panel detection and control	O 3.3V	PU 2k2 3.3V	
FPDDC_DAT DDC	Lines used for flat panel detection and control	I/O 3.3V	PU 2k2 3.3V	

Signal	Description	I/O	Termination	Remarks
IDE_D0-15	Primary IDE Data bus	I/O 3.3V		5V tolerant
IDE_A0-2	Primary IDE Address bus	O 3.3V		
IDE_CS1#	Primary IDE chip select channel 0	O 3.3V		
IDE_CS3#	Primary IDE chip select channel 1	O 3.3V		
IDE_DRQ	Primary IDE DMA request	I 3.3V		5V tolerant
IDE_DACK#	Primary IDE DMA acknowledge	O 3.3V		
IDE_RDY	Primary IDE ready	I 3.3V	PU 4k7 3.3V	5V tolerant
IDE_IOR#	Primary IDE IO read	O 3.3V		
IDE_IOW#	Primary IDE IO write	O 3.3V		
IDE_INTRQ	Primary IDE interrupt request	I 3.3V	PU 8k2 3.3V	5V tolerant
DASP	IDE Drive active			NC
PDIAG	IDE Master/Slave negotiation	NC		
IDE_RST#	Hard Drive reset	O 5V		

Signal	Description	I/O	Termination	Remarks
RSMRST#	Resume / reset input	I 3.3VSB	PU 100k 3.3VSB	
SMBALRT#	System management bus alert in	I 3.3VSB	PU 100k 3.3VSB	
BATLOW#	Battery low input	I 3.3VSB	PU 100k 3.3VSB	
GPE1#	General purpose power management event input 1	I 3.3VSB	PU 100k 3.3VSB	
GPE2#	General purpose power management event input 2	I 3.3VSB	PU 100k 3.3VSB	
EXTSMI#	System management interrupt input	I 3.3VSB	PU 100k 3.3VSB	
PWGIN	Power good input	I		Also usable as a reset input; make low with O.C. to cause reset
5V_ALW	Supply of internal suspend circuit	Power-In		Input voltage of the SMX
PS_ON#	Power Save ON	O 5VSB	10k 5VSB	
PWRBTN#	Power Button	I 5VSB	10k 5VSB	
I2CLK	I2C Bus clock	I/O 5V	PU 10k 5V	
I2DAT	I2C Bus Data	I/O 5V	PU 10k 5V	
SMBCLK	SM Bus clock	I/O 3.3V	PU 2k2 3.3V	
SMBDATA	SM Bus Data	I/O 3.3V	PU 2k2 3.3V	

6.7. Signal Integrity Requirements

The signal groups listed in the following table have signal-integrity concerns that should be accounted for in module and carrier board designs. A general description is shown in the table for reference only. The designer should consult the relevant interface specification documents for complete information.

Signal Group	General Description	Source Spec Reference
Analog VGA	75-ohm single ended ground-referenced lines. Generous isolation recommended.	
Component and Composite video	75-ohm single ended ground-referenced lines. Generous isolation recommended.	
Gigabit Ethernet	Differential pairs	IEEE 802.3 Specification
LVDS	100-ohm edge coupled differential pairs	National Semiconductor LVDS web site
PCI Bus	Circa 60 ohm single-ended	PCI SIG - PCI Local Bus Spec. Rev. 2.3
PCI and LPC clocks	50-ohm single ended ground-referenced	
PCI Express	Differential pairs	PCI SIG - PCI Express Specification
PCI Express clocks	100 ohm edge couple differential pair, ground-referenced	
Serial ATA	Differential pairs	SATA Specification
USB	Differential pairs	USB 2.0 Specification

6.8. Thermal Specifications

** To be determined.

7. Design Rules for the Integration

On this product, there are many very fast interfaces. Some of these interfaces work differentially and must be routed in twisted pair with equal flight times. All power signals must be designed as power planes including all decoupling capacitors. The power planes and their vias must be capable of transporting the maximum energy.

7.1. Video Signals

The DAC channel (red, green, blue) outputs should be routed as single-ended shielded routes. An analog switch should be used in order to provide the proper termination that is required for high-performance video signal integrity. The analog switch should exhibit a low "on" resistance (< 8) and low parasitic capacitance (<10 pF). The output routing from the analog switch should be routed as single-ended 37.5- impedance to the 75- termination resistors that are located near the VGA connector on the motherboard and the VGA connector on the docking station. The single- ended routing after these 75- termination resistors to the pi-filter and then to the VGA connector should ideally be 75.

HSYNC and VSYNC signals are connected to the analog display attached to the VGA connector. These are 3.3-V outputs from the GMCH. A 39 Ohm series resistor is required before routing to the VGA connector. Also, capacitors (28 pF - 33 pF) before and after the series resistor may be needed to meet the VESA rise/fall time specification.

Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

DDCADATA and DDCACLK are 3.3-V IO buffers connecting the GMCH to the monitor. If higher signaling voltage (5 V) is required by the monitor, level shifting devices may be used. Pull-up resistors of 2.2-k (or the appropriate value derived from simulation) are required on each of these signals.

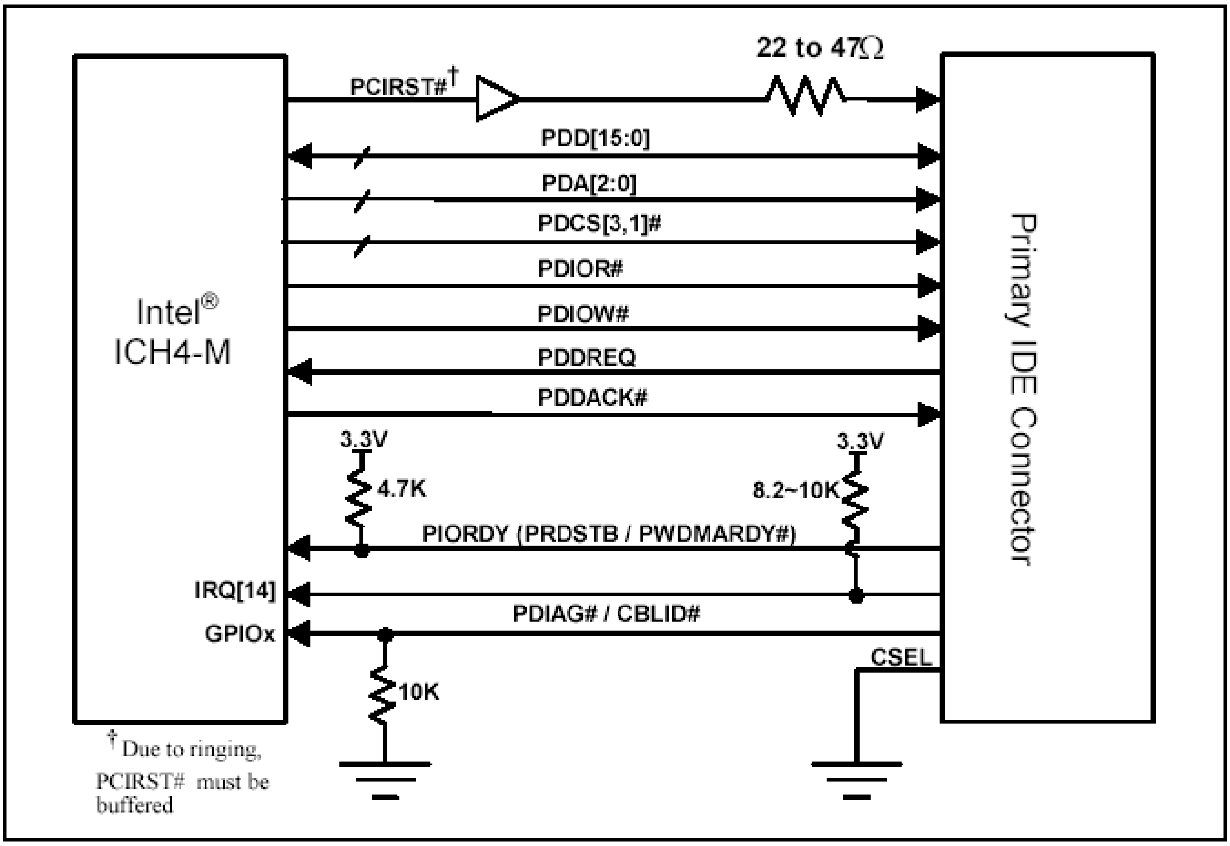
LVDS Signals:

Signal Group	LVDS
Topology	Differential
Referred plane	Ground
Impedance	100 Ohm +/-15%
Trace with / pair spacing	4mil / 7mil
Number of allowed vias	2
Maximal length	20cm
Length matching	+/- 1mm
Remarks:	-

DVO Signals:

Signal Group	DVO
Topology	Data: single Clocks: differential
Referred plane	Ground
Impedance	55 Ohm +/-15%
Trace with / pair spacing	4mil / 8mil
Number of allowed vias	2
Maximal length	10cm
Clock length matching	Data: +/- 10mm Clocks: +/- 1mm
Remarks:	-

7.2. IDE Signals



Signals:

Follow these connection requirements for an IDE connector:

- 22-47 series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 to 10 k pull-up resistor is required on IRQ14 to VCC3_3.
- A 4.7kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.
- Series resistors of 10 Ohms can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
- The 10kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

Place a 22uF/10V capacitor at each power pin of the interface connector.

7.3. AC97 Audio Signals

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground plane, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. This means that no signal should cross the EMI emissions thus degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

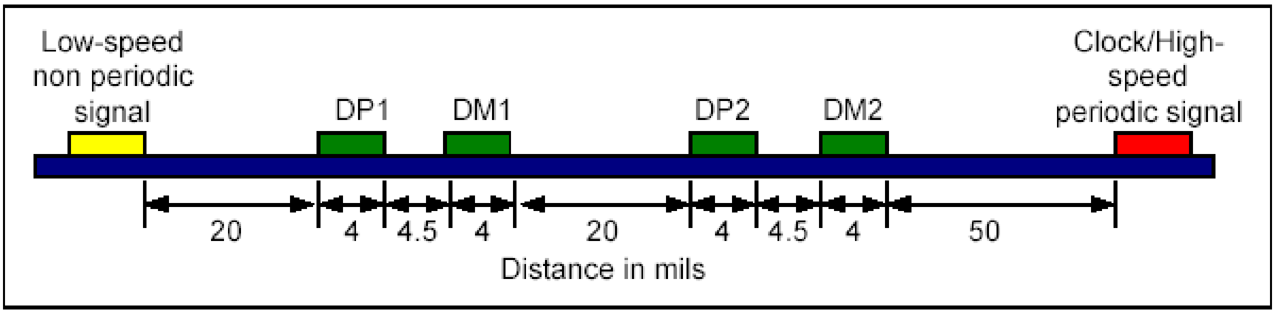
7.4. USB2 Signal

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in the placement of most of the routing on the fourth plane (closest to the ground plane), allowing a higher component density on the first plane.

1. Place the ICH7-M and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
2. USB 2.0 signals should be ***ground referenced***.
3. Route USB 2.0 signals using a minimum of vias and corners.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
5. Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
6. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs for a particular line should not be greater than 200 mils.
7. Route all traces over continuous planes (VCC or GND), with no interruptions. If at all possible, avoid crossing over anti-etch.
8. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
9. Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
10. Place a 10uF/10V tantalum capacitor and a 100nF capacitor directly at the power pin of each USB2 connector.

USB Signals:

Signal Group	USB2
Topology	Differential
Referred plane	Ground
Impedance	90 Ohm +/-15%
Trace with / pair spacing	4mil / 4.5mil
Number of allowed vias	2
Maximal length	20cm
Length matching	+/- 0.5mm
Remarks:	-



7.5. LAN Signals

Component placement can affect signal quality, emissions, and temperature of a board design.

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC.
- Simplify the task of routing traces. To some extent, component orientation will affect complexity of trace routing. The overall objective is to minimize turns and crossovers.

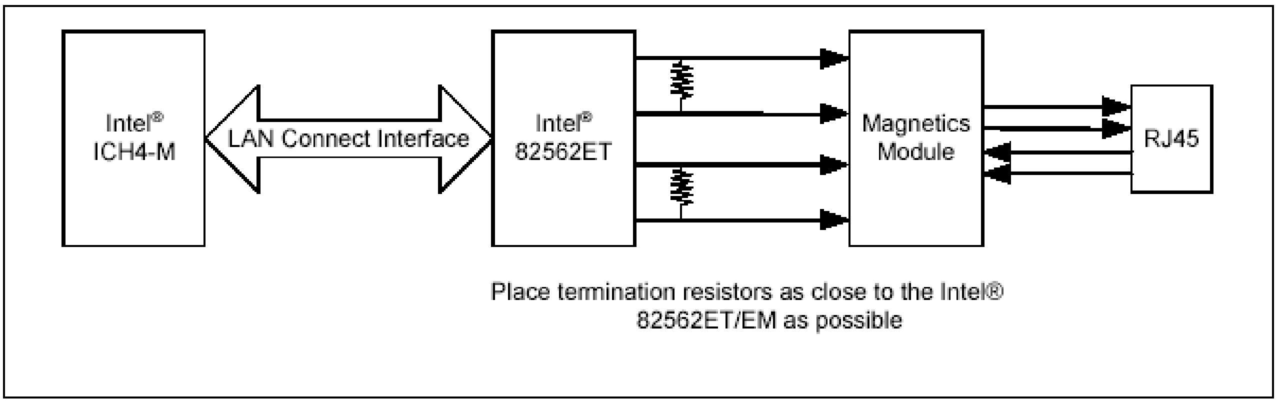
Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis.

Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal, if they exist, should be grounded to prevent possible radiation from the crystal case. The crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board. For a noise free and stable operation, place the crystal and associated discrete components as close as possible to the Intel 82562ET/EM, keeping the trace length as short as possible and do not route any noise signals in this area.

The 100 Ohms ± 1% resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ohms ± 1% receive differential pairs (RDP/RDN) and should be placed as close to the platform LAN connect component (Intel 82562ET or Intel 82562EM) as possible. This is due to the fact that these resistors are terminating the entire impedance that is seen at the termination source (i.e. Intel 82562ET).

LAN Signals:

Signal Group	LAN
Topology	Differential
Referred plane	Ground
Impedance	55 Ohm +/-1%
Trace with / pair spacing	4mil / 7mil
Number of allowed vias	2
Maximal length	20cm
Length matching	+/- 1mm
Remarks:	-

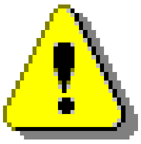


7.6. Power Planes

Use a plane for all power signals. Place decoupling capacitors on each power plane as referred to in the following table:

Power Plane for Power Input to the SMX945	Voltage (Volt)	Current (Amp)	Voltage Tolerance	Decoupling Capacitors
DCIN 12V For generating the processor core voltage	12V (5V-18V)	30Watt	- (internal reg)	10x 22uF/35V CER LowESR 5x 1uF/35V CERCAP 2x 2200uF/35V
VCC5ALW	5.0V	0.1A	+/- 5%	5x 100nF

The VCC3, VCC3ALW and VCC5 are generated internally on the SMX945 module.



Attention!
The minimum input voltage is 4.9Volt under full load. Be careful that the power plane is able to support 8Amp peaks with a voltage loss of not more than 100mV.

Power Output from the SMX945

Power Plane from the SMX945 to supply circuits on the motherboard	Voltage (Volt)	Current (Amp)	Voltage Tolerance	Decoupling Capacitors
VCC3ALW	3.3V	0.05	+/-5%	Only for test purposes
VCC3	3.3V	0.1	+/-5%	Only for test purposes

8. DETAILED SPECIFICATIONS



Note...
On the following pages are design-in recommendations taken from various Intel manuals.

8.1. Intel Core Duo Processors

Intel® Core™ Duo processors run at different voltage/frequency states (performance states), which is referred to as Enhanced Intel® SpeedStep® technology (EIST). Operating systems that support performance control take advantage of microprocessors that use several different performance states in order to efficiently operate the processor when it is not being fully utilized.

The operating system will determine the necessary performance state that the processor should run at so that the optimal balance between performance and power consumption can be achieved during runtime. The Windows family of operating systems links its processor performance control policy to the power scheme setting found in the control panel option applet.

If the “Home/Office” or “Always On” power scheme is selected when using Windows operating systems, then the processor will always run at the highest performance state. For more information about this subject see Chapter 8 of the ACPI Specification Revision 2.0c, which can be found at www.acpi.info . Also, visit Microsoft's website and search for the document called “Windows Native Processor Performance Control”.

The BIOS allows you to limit the maximum processor frequency. This can be useful if the maximum performance is not required or if the maximum processor performance state dissipates too much power and heat.

In the “CPU Configuration” submenu of the “BIOS Setup Program” you'll find the node for “Max. Frequency” limitation. For each Intel® Core™ Duo processor, the BIOS lists the supported frequencies. If a lower frequency than the maximum one is selected, the processor will never run at frequencies above this setting.

Celeron M processors do not support Enhanced Intel® SpeedStep® technology; they always run at a fixed frequency. In order to limit the performance and power consumption of Celeron M processors, the BIOS offers “On-Demand Clock Modulation” support in the “CPU Configuration” submenu of the “BIOS Setup Program”.

When “On-Demand Clock Modulation” is enabled, the processor clock is throttled using the duty cycle determined in setup. Keep in mind that the “On-Demand” clock modulation duty cycle indicates the clock-on to clock-off interval ratio. This means that when set to 75% the clock is running 75% of the overall time and leads to a performance decrease of approximately 25%.

With the Celeron M 440 (1.86GHz CPU), the power consumption decreases approximately 3W when set to 75% duty cycle and 6W when set to 50% duty cycle.

8.2. Thermal Monitor and Catastrophic Thermal Protection

Intel® Core™ Duo processors have a thermal monitor feature that helps to control the processor temperature. The integrated TCC (Thermal Control Circuit) activates if the processor silicon reaches its maximum operating temperature. The activation temperature that the Intel Thermal Monitor uses to activate the TCC cannot be configured by the user nor is its software visible. The Thermal Monitor can control the processor temperature through the use of two different methods defined as TM1 and TM2. The TM1 method consists of the modulation (starting and stopping) of the processor clocks at a 50% duty cycle. The TM2 method initiates an Enhanced Intel® SpeedStep® transition to the lowest performance state once the processor silicon reaches the maximum operating temperature.

The maximum operating temperature for Intel® Core™ Duo processors is 100°C. TM2 mode is used for Intel® Core™ Duo processors. Two modes are supported by the Thermal Monitor to activate the TCC. They are called Automatic and On-Demand. No additional hardware, software, or handling routines are necessary when using Automatic Mode.

To ensure that the TCC is active for only short periods of time, thus reducing the impact on processor performance to a minimum, it is necessary to have a properly designed thermal solution. The Intel® Core™ Duo processor's datasheet can provide you with more information about this subject.

The THERMTRIP# signal is used by the Intel® Core™ Duo processors for catastrophic thermal protection. If the processor's silicon reaches a temperature of approximately 125°C then the processor signal THERMTRIP# will go active and the system will automatically shut down to prevent any damage to the processor as a result of overheating. The THERMTRIP# signal activation is completely independent from processor activity and therefore does not produce any bus cycles.

In order for THERMTRIP# to be able to automatically switch off the system it is necessary to use an ATX-style power supply.

8.2.1. Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

8.2.2. The SMX945 ACPI Thermal Solution

The SMX945 ACPI Thermal Solution offers three different cooling policies:

8.2.2.1. Passive Cooling

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the “passive cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

8.2.2.2. Active Cooling

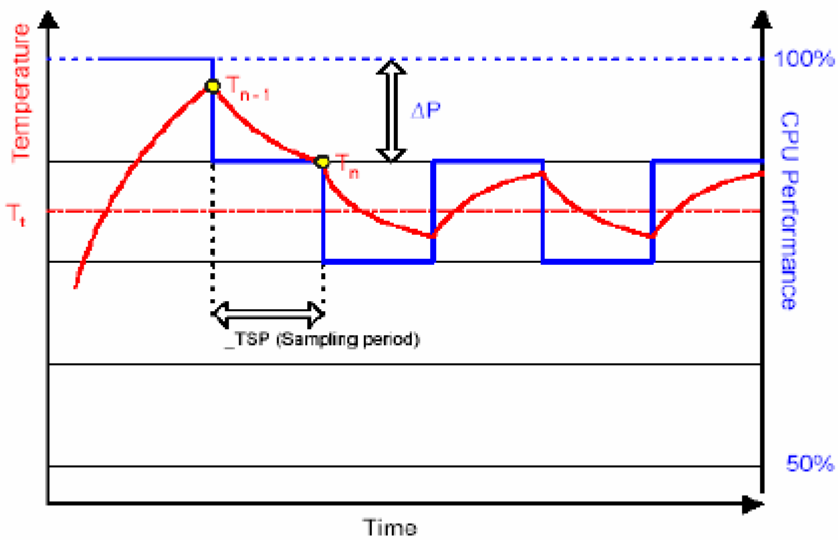
During this cooling policy the operating system is turning the fan on/off. Although active cooling devices consume power and produce noise, they also have the ability to cool the thermal zone without having to reduce the overall system performance. Use the “active cooling trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the active cooling device.

8.2.2.3. Critical Trip Point

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as a result of high temperatures. Use the “critical trip point” setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.

8.2.3. Implementation

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points. If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled according to the formula below.



ΔP[%] = TC1(Tn-Tn-1) + TC2(Tn-Tt)

ΔP is the performance delta.
Tt is the target temperature = critical trip point.
The two coefficients, TC1 and TC2, and the sampling period (TSP) are hardware-dependent constants. These constants are set to fixed values for the SMX945:

TC1 = 1 TC2 = 5 TSP = 5sec.

8.3. ACPI Suspend Modes and Resume Events

The SMX945 supports the S1 (POS = Power On Suspend) and S3 (STR = Save to RAM) states. S4 (Save to Disk) is not supported by the BIOS (S4_BIOS) but is supported by the following operating systems (S4_OS = Hibernate):

- Win2K
- WinXP

The following table lists the "Wake Events" that resume the system from both S1 or S3 unless otherwise stated in the "Conditions/Remarks" column.

Wake Event	Conditions/Remarks
Power Button	Wakes unconditionally from S1-S5
GPE1#	Only if configured as Lid Switch in the ACPI setup menu. Additionally the lid button has to be activated using the Windows Power Options. The best way to use it is to go to Standby on lid button, press and wake from Standby on lid button release.
GPE2#	Set GPE2 Function node to Sleep Button in the ACPI setup menu or set Resume On Ring to Enabled in the Power setup menu.
Onboard LAN Event	Device driver must be configured for Wake On LAN support. For configuration go to Device Manager, Network Adapters, Intel(R) PRO/100 VE Network Connection and launch properties. Power Management: Allow this device to bring the computer out of standby. Advanced → Wake on LAN Options → Properties: Enable PME:Enabled Wake On Link Settings: Forced Wake On Settings: Wake on Magic & Directed Using this configuration the system will wake from Standby in case a magic packet or a directed packet is sent. Directed packet: e.g. ping to last IP / MAC address. If there is no network cable connected to the system when it goes to Standby mode, the system will wake from Standby as soon as a cable is connected.
SMBALERT#	Wakes unconditionally from S1-S5
PCI Express WAKE#	Wakes unconditionally from S1-S3
PME#	Activate the wake up capabilities of a PCI device using Windows Device Manager configuration options for this device **or** set Resume On PME# to Enabled in the Power setup menu.
USB Mouse/Keyboard Event	When Standby mode is set to S1, no special action must be taken for a USB Mouse/Keyboard Event to be used as a Wake Event. When Standby mode is set to S3, the following must be done for a USB Mouse/Keyboard Event to be used as a Wake Event: USB Hardware must be powered by standby power source. Set USB Device Wakeup from S3/S4 to ENABLED in the ACPI setup menu. Under Windows XP add following registry entries: Add this key: HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\usb Under this key add the following value: "USBBIOSx"=DWORD:00000000
RTC Alarm	Activate and configure Resume On RTC Alarm in the Power setup menu
Watchdog Power Button Event	Wakes unconditionally from S1-S5
PS/2 Mouse/Keyboard Event	Only can be used as a Wake Event when in S1 mode

Note...
Windows XP disables USB wakeup from S3, so this entry has to be added to re-enable it.

Configure USB keyboard/mouse to be able to wake up the system:

In Device Manager look for the keyboard/mouse devices. Go to the Power Management tab and check "Allow this device to bring the computer out of standby".



Note…
When the standby state is set to S3 in the ACPI setup menu, the power management tab for USB keyboard /mouse devices only becomes available after adding the registry entry (see the table on previous page) and rebooting to allow the registry changes to take affect.

8.4. PCI Resources

Addressing PCI devices on the SMX945:

DEVICE	IDSEL	PIRQ	#REG	#GNT	Remarks
Internal Chipset PCI devices and resources					
GMCH	internal		---	---	PCI Bus 0
PEG Controller	internal		---	---	PCI Bus 0
Graphics Controller	internal		---	---	PCI Bus 0
ICH7_USB Controller	Internal		---	---	PCI Bus 0 Func 0 = USB0 mapped to PIRQH Func 1 = USB1 mapped to PIRQD Func 2 = USB2 mapped to PIRQC Func 3 = USB3 mapped to PIRQA Func 7 = USB2.0 mapped to PIRQH
ICH7_HUB Controller	internal		---	---	PCI Bus 0 AC97 Audio mapped to PIRQB AC97 Modem mapped to PIRQE
ICH7_LPC Controller			---	---	PCI Bus 0 IDE mapped to PIRQC SATA mapped to PIRQD SMBUS mapped to PIRQD CHAP mapped to PIRQA
ICH7_AZALIA Controller	internal				PCI Bus 0
ICH7_PCIE Controller	internal		---	---	PCI Express Ports 1-4 Slot1 mapped to PIRQB Slot2 mapped to PIRQA Slot3 mapped to PIRQC Slot4 mapped to PIRQD
Network	internal AD24		---	---	PCI Bus 6 Internal chipset onboard device
External PCI slots					
PC/104+ Slot 1	AD20	E / F / G / H	0-4	0-4	PCI Bus 6
PC/104+ Slot 2	AD21	F / G / H / E	0-4	0-4	PCI Bus 6
PC/104+ Slot 3	AD22	G / H / E / F	0-4	0-4	PCI Bus 6
PC/104+ Slot 4	AD23	H / E / F / G	0-4	0-4	PCI Bus 6

9. CORE BIOS

For BIOS specific information, please refer to the driver/software/BIOS manual “SMX945_BIOS” on the Product CD.

Examples of BIOS specific information: Core BIOS Download, BIOS History, The Special Function Interface (SFI), Console Redirection, etc.

10. SCHEMATICS

You will find the schematics of the MSEBX945 on the SMX945 Product CD.

MSEBX945 V1.0

12.04.2007 DIGITAL-LOGIC AG

History for MSEBX945CX

V0.1 Initial Draft 1.12.06 BAM
V1.0 PCI104Express specification 0.6B
PCI104Express Connector on Bottom Side added
SATA2 changed on COM-Express
SATA3 & SATA 4 added
100MB LAN from Module compatible for 1GB

PCI - Resources	IRQ#	ID_SEL	GNT# / REQ#
EXAR for 4serial COM-Ports	B	AD_26	--
Frame Grabber BT878	D	AD_19	4 / 4
Mini PCI-Slot	A / B	AD_27	3 / 3
PC104+ / A Slot	E	AD_20	0 / 0
PC104+ / B Slot	F	AD_21	1 / 1
PC104+ / C Slot	G	AD_22	2 / 2
PC104+ / D Slot	H	AD_23	3 / 3

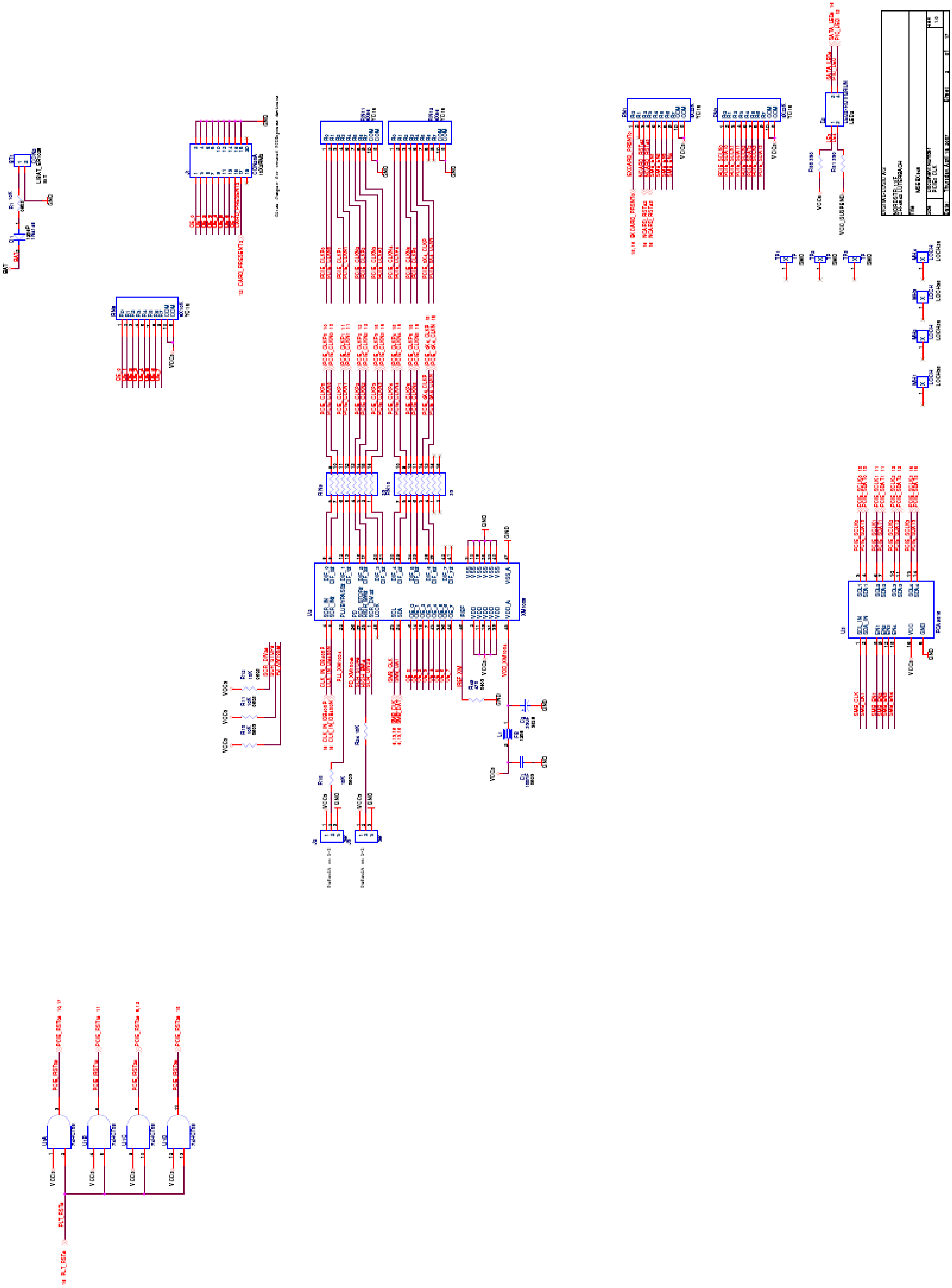
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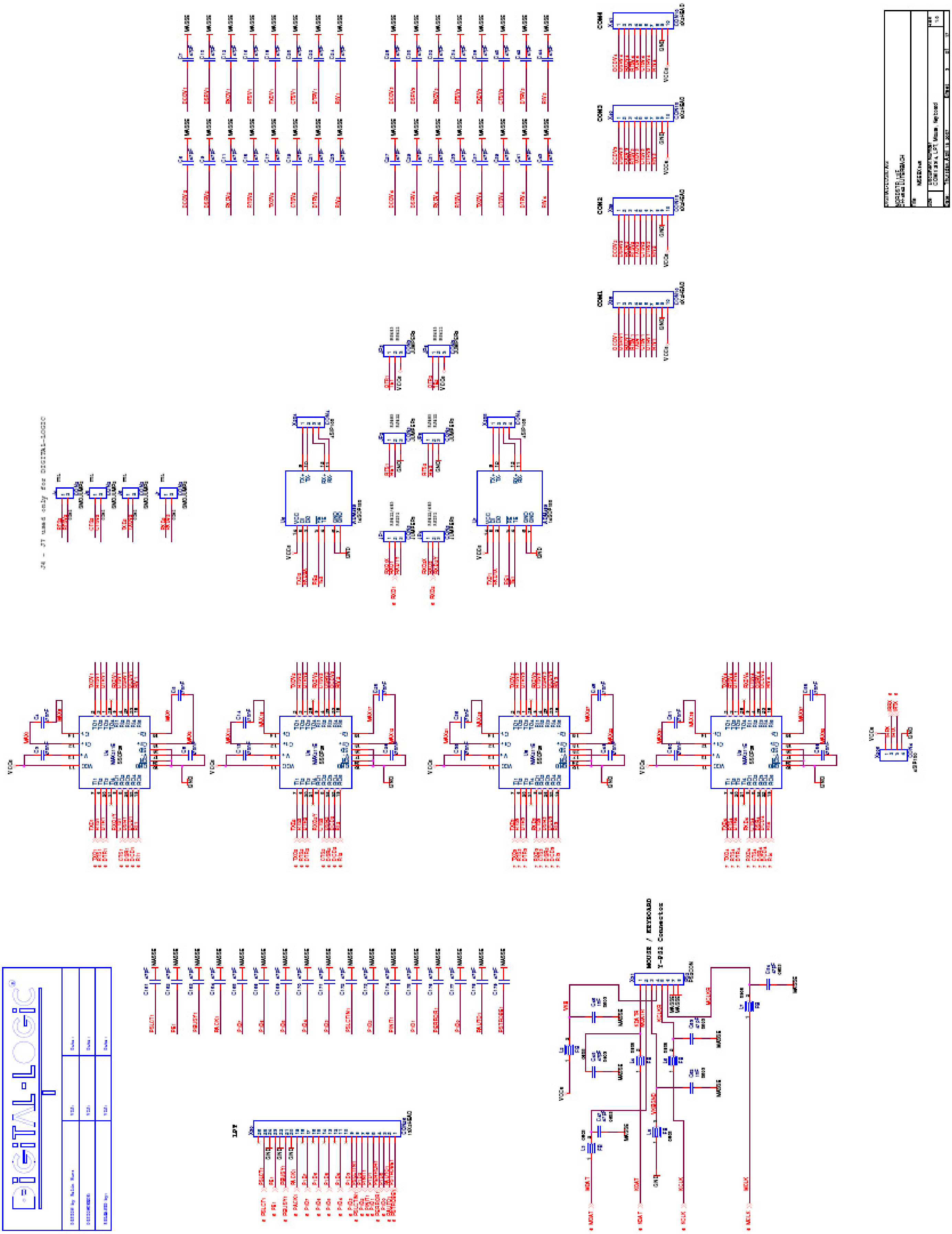
PENTIUM-M MICROSPACE

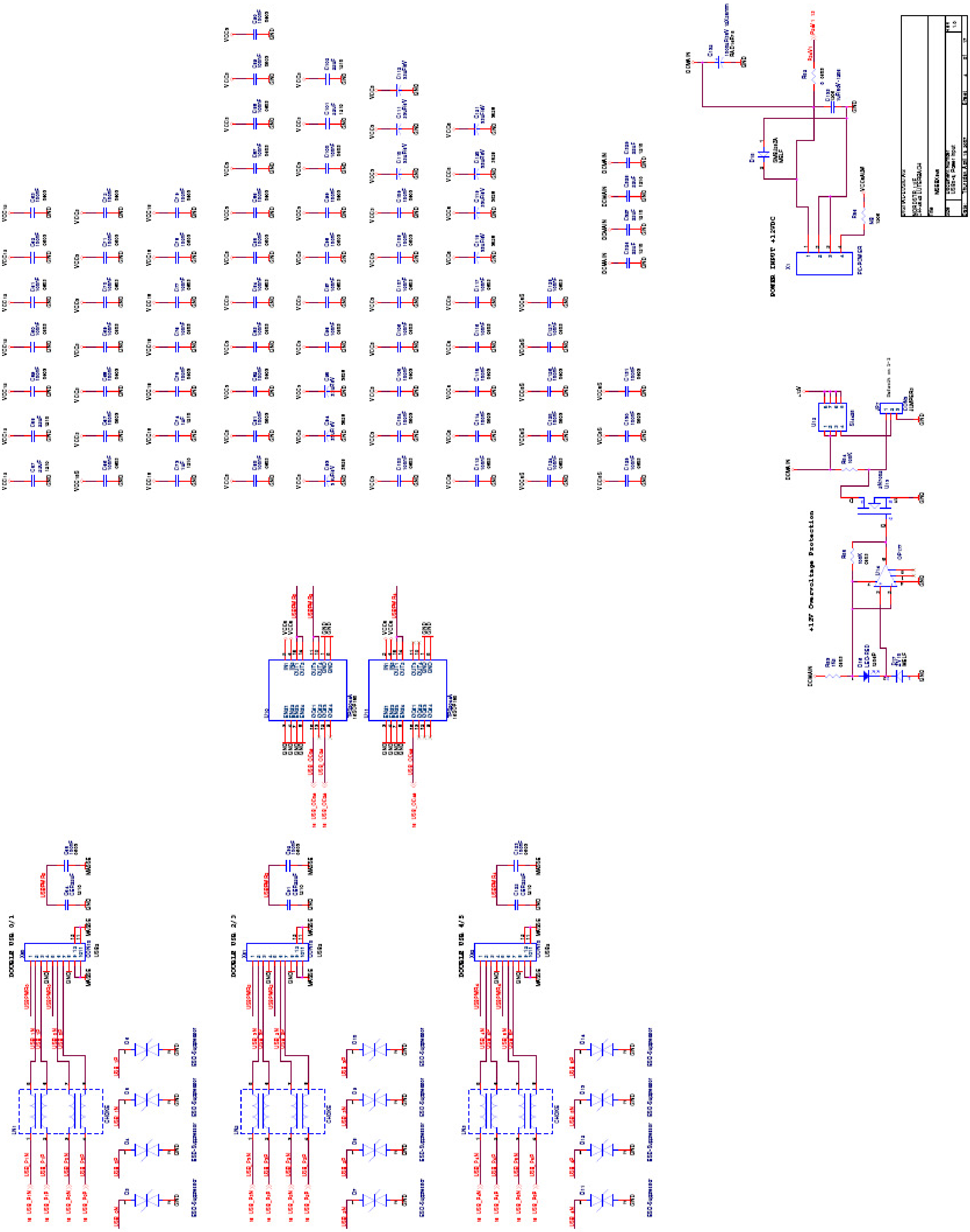
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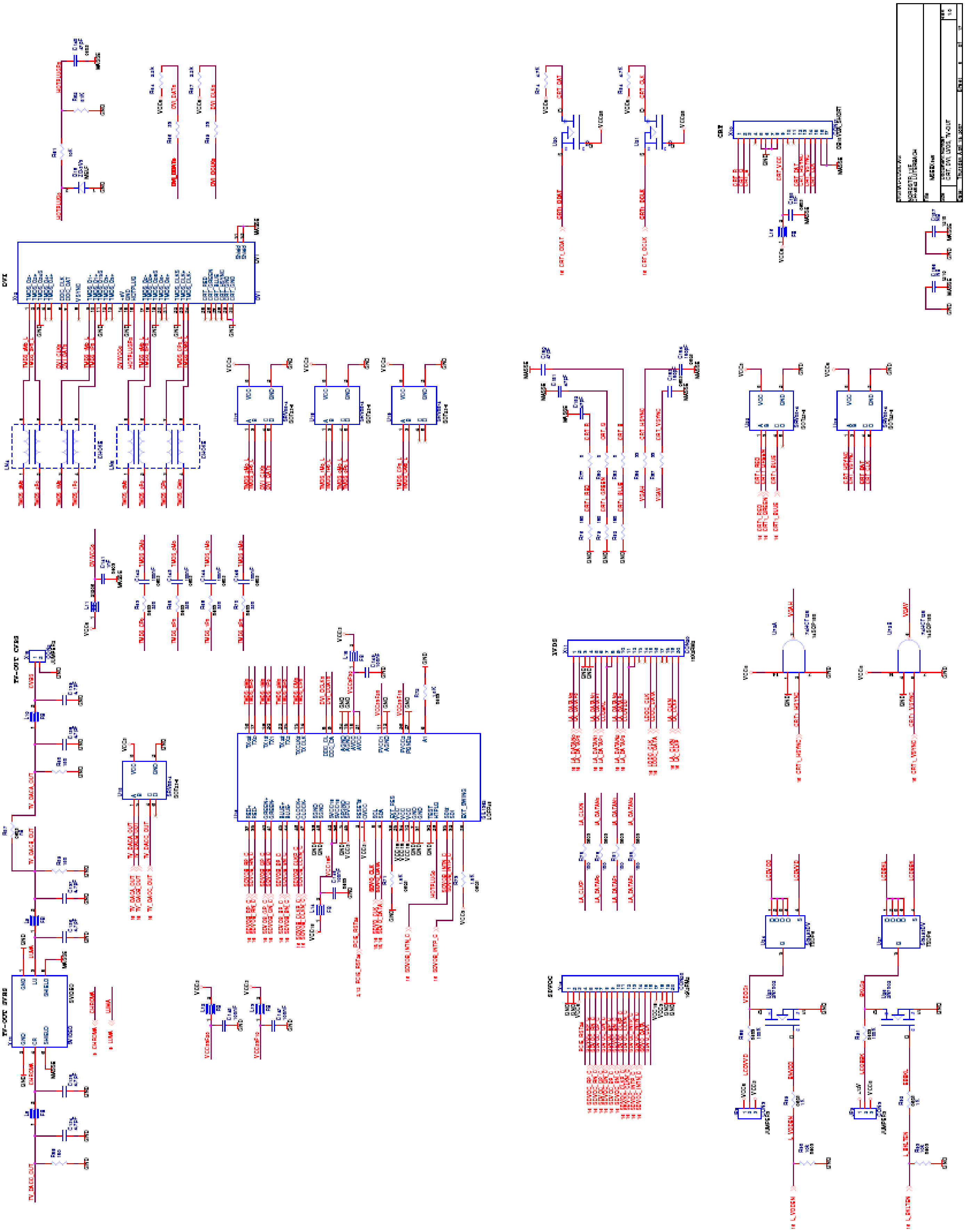
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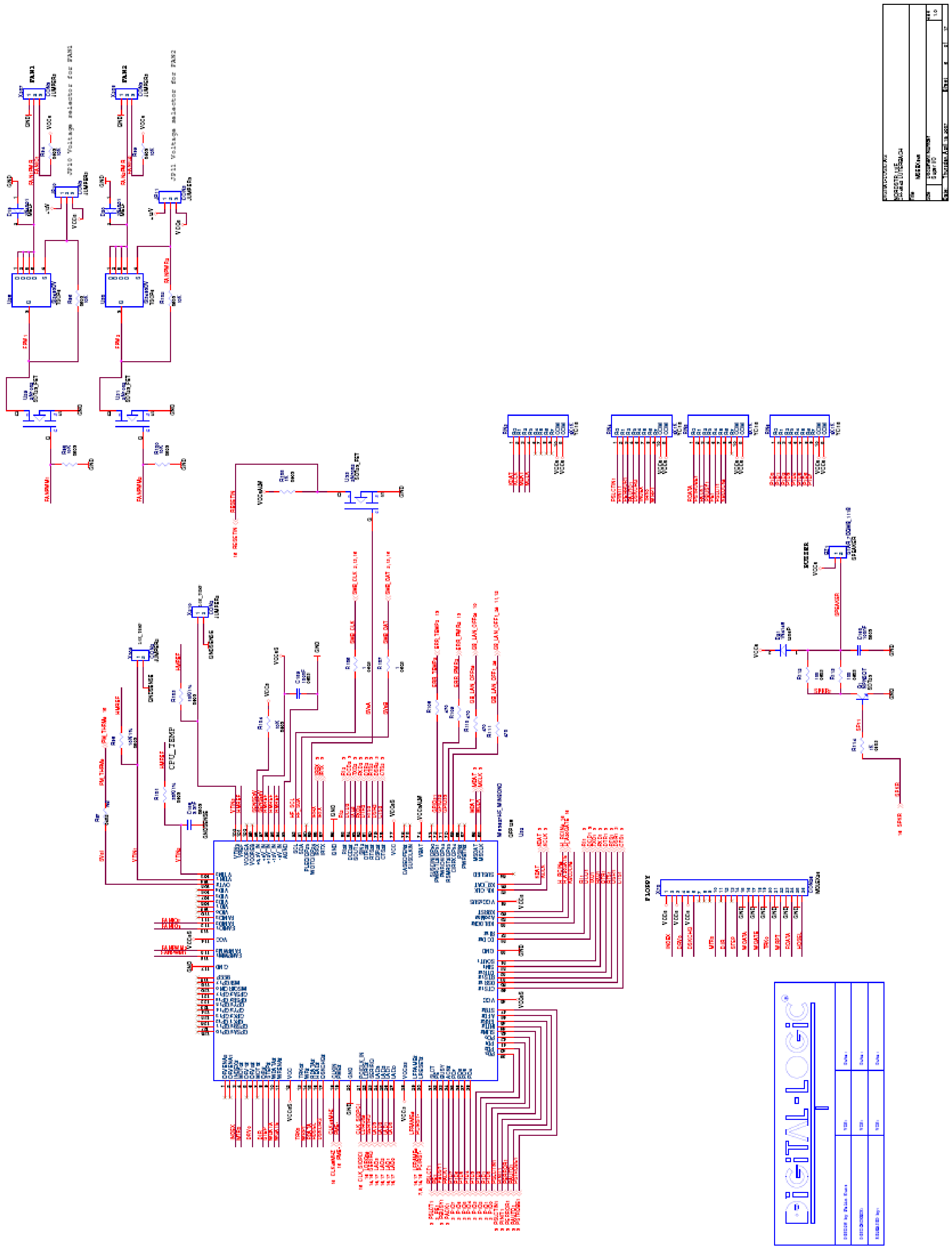
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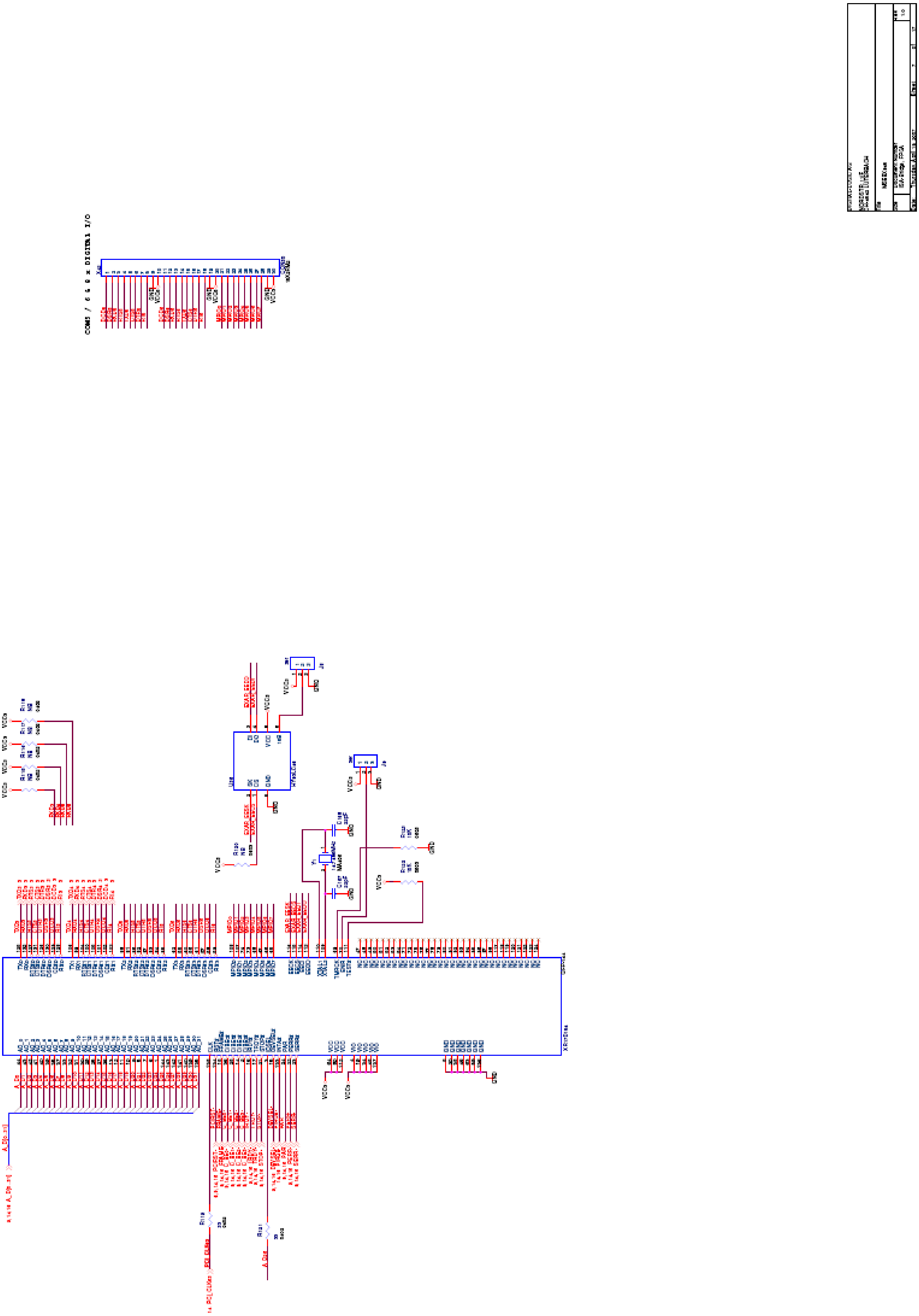


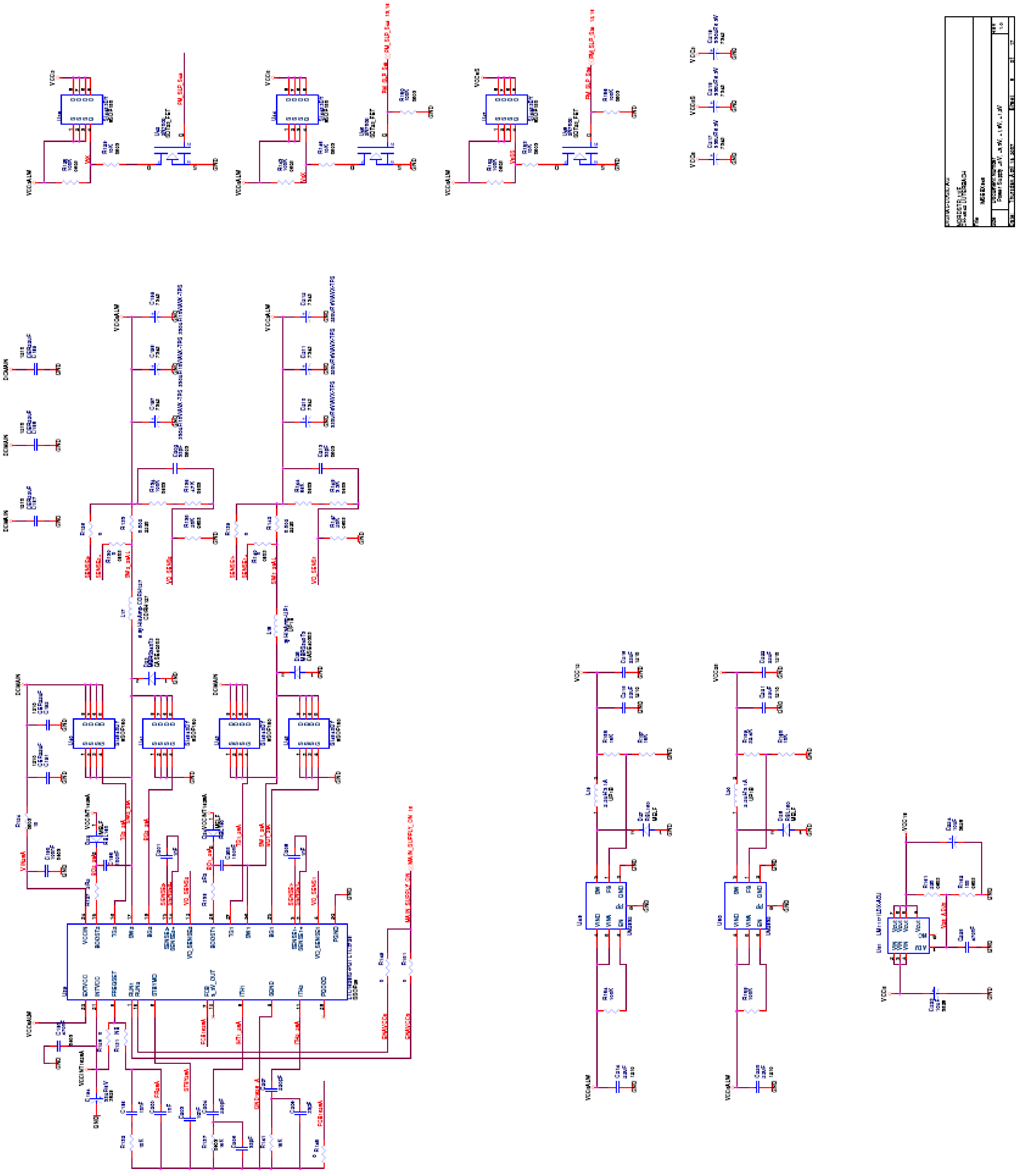


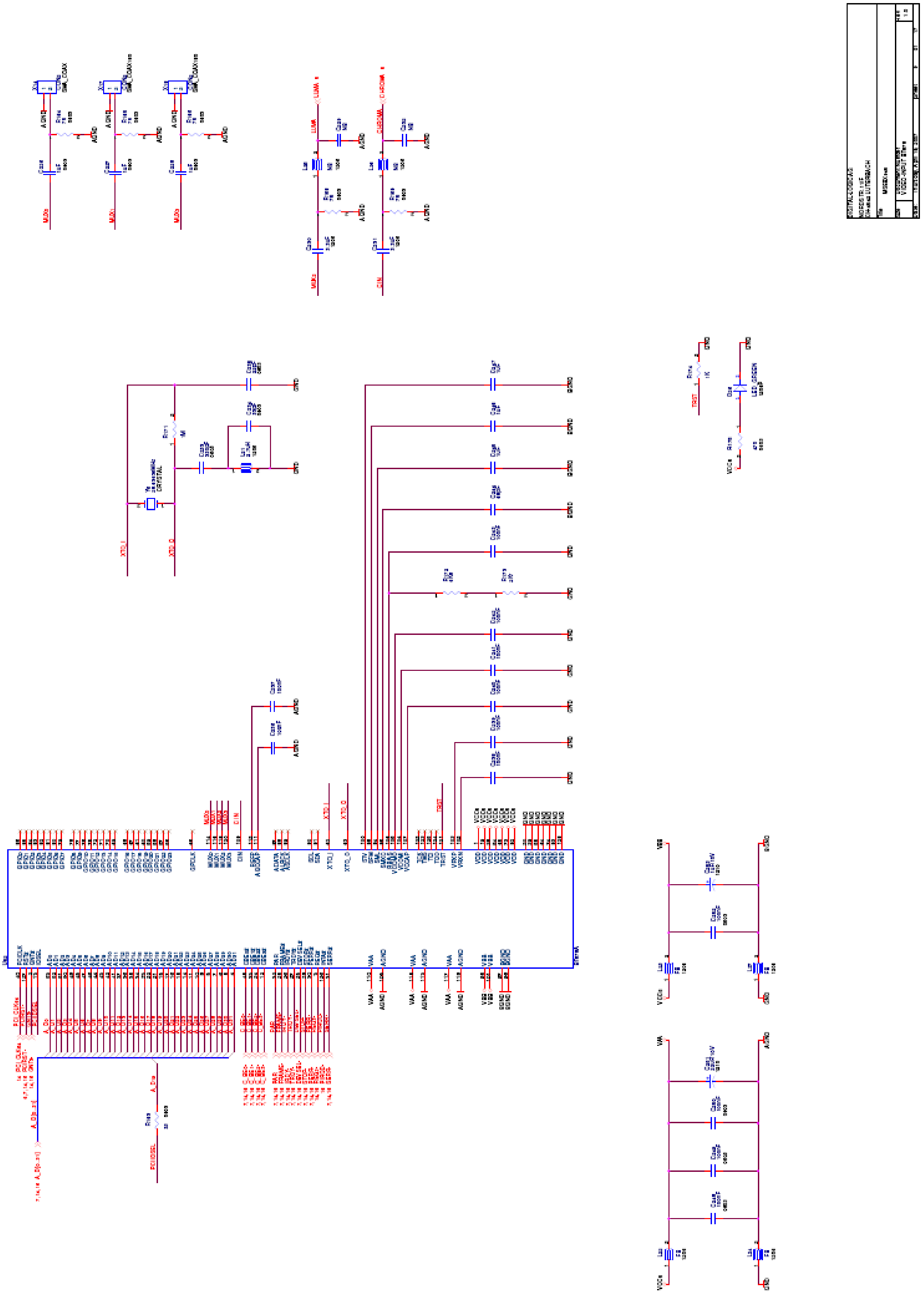

POWER INPUT +12VDC
+12V Overvoltage Protection
DOUBLE USB 0/1
DOUBLE USB 2/3
DOUBLE USB 4/5

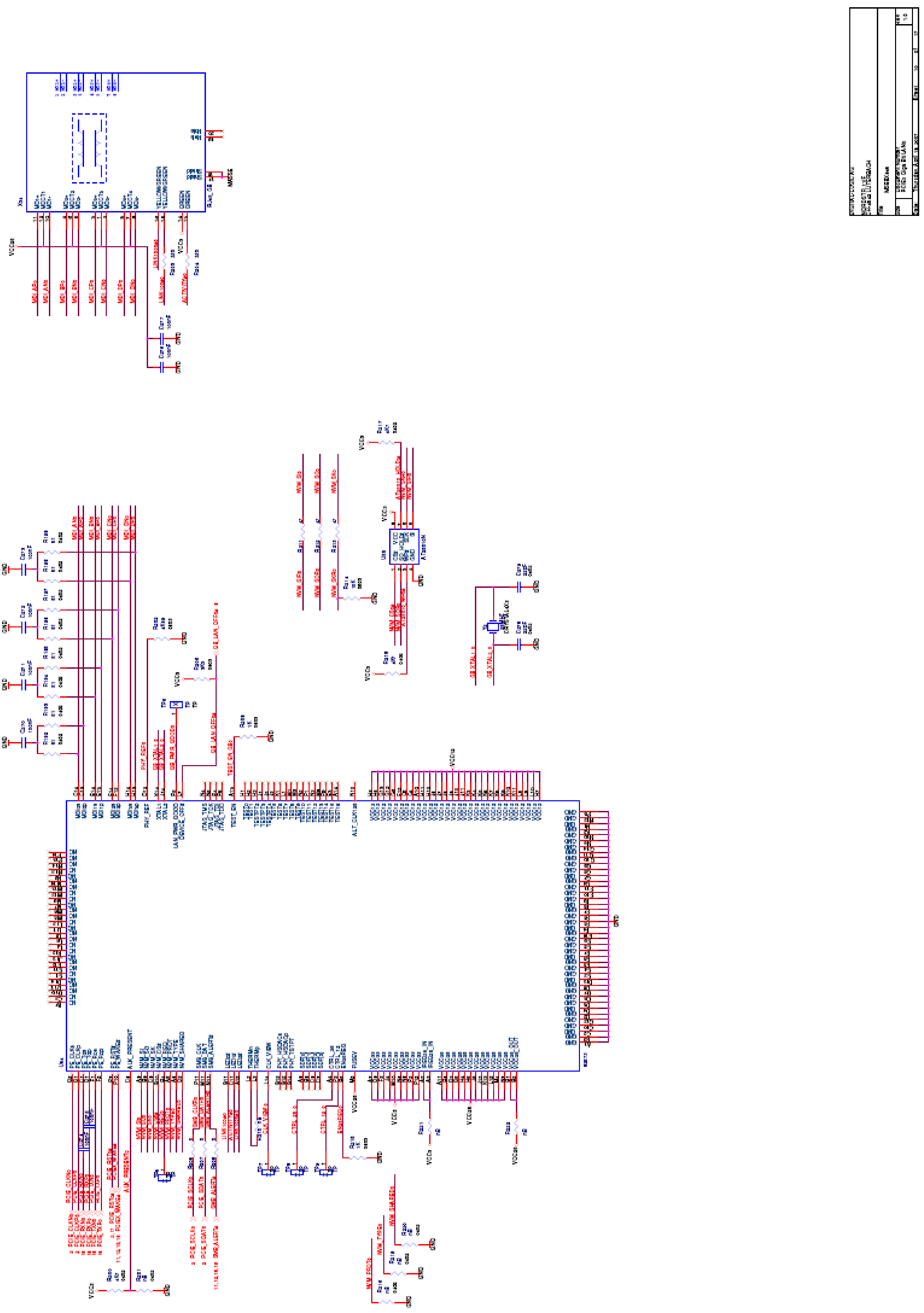


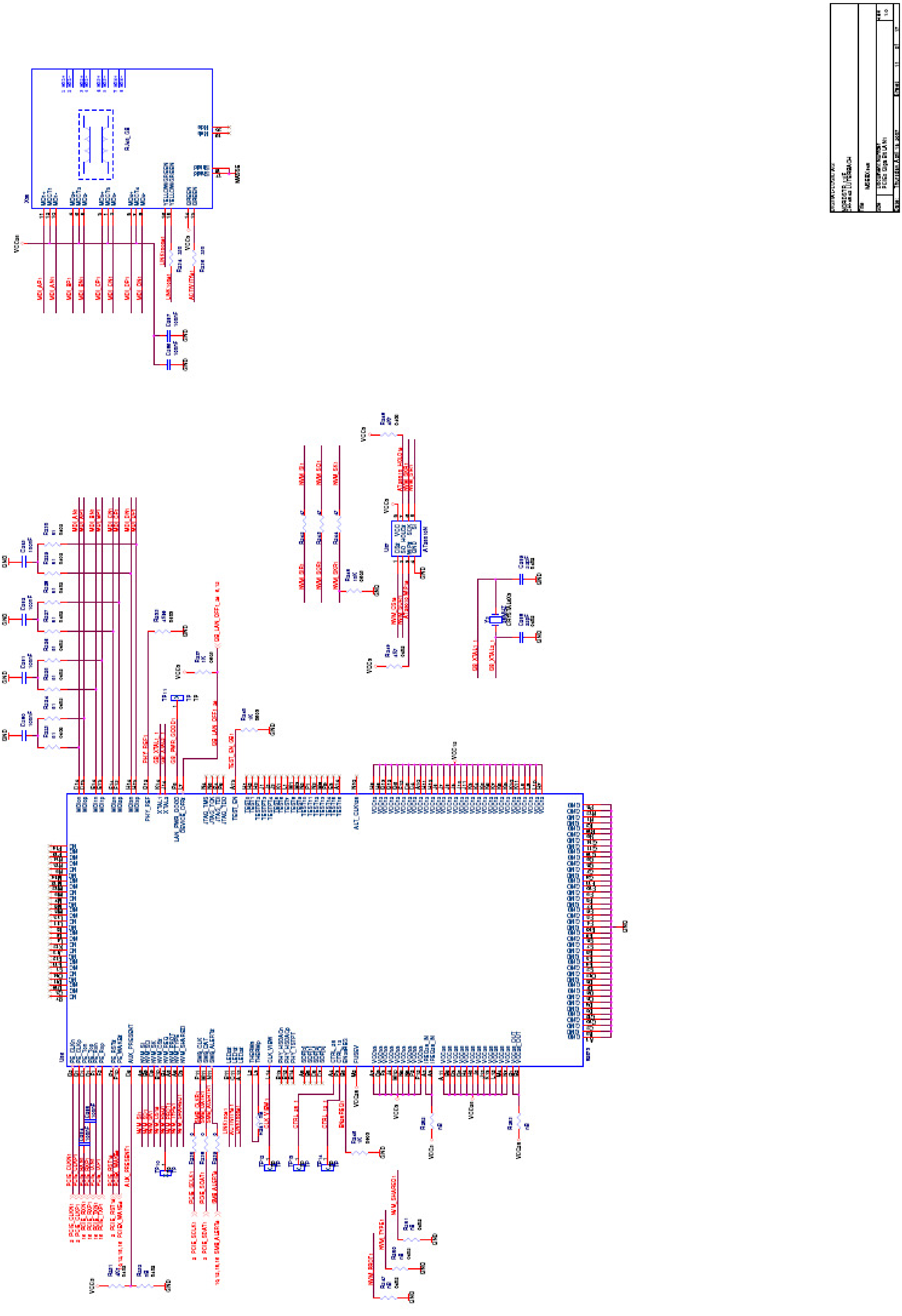


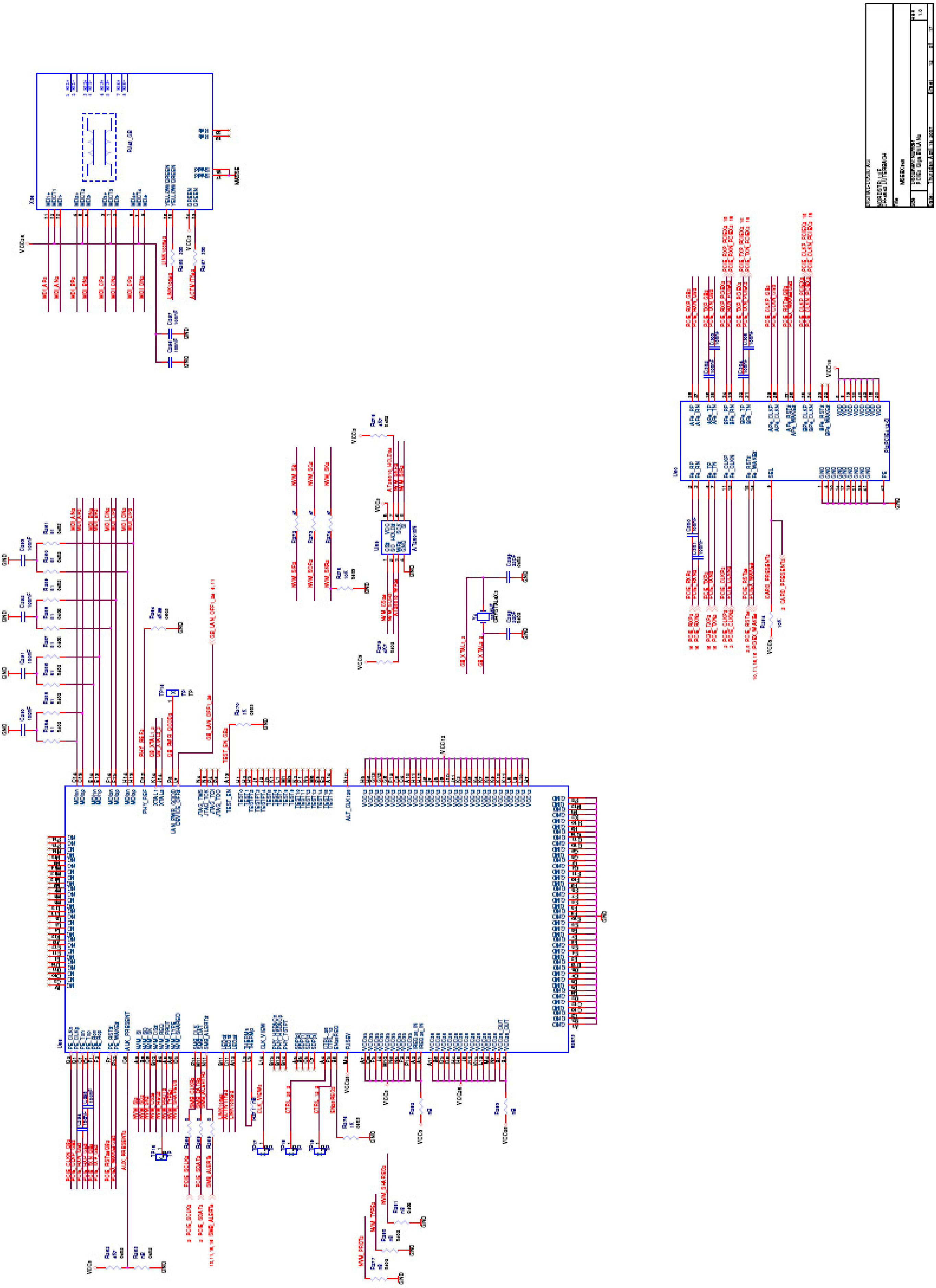


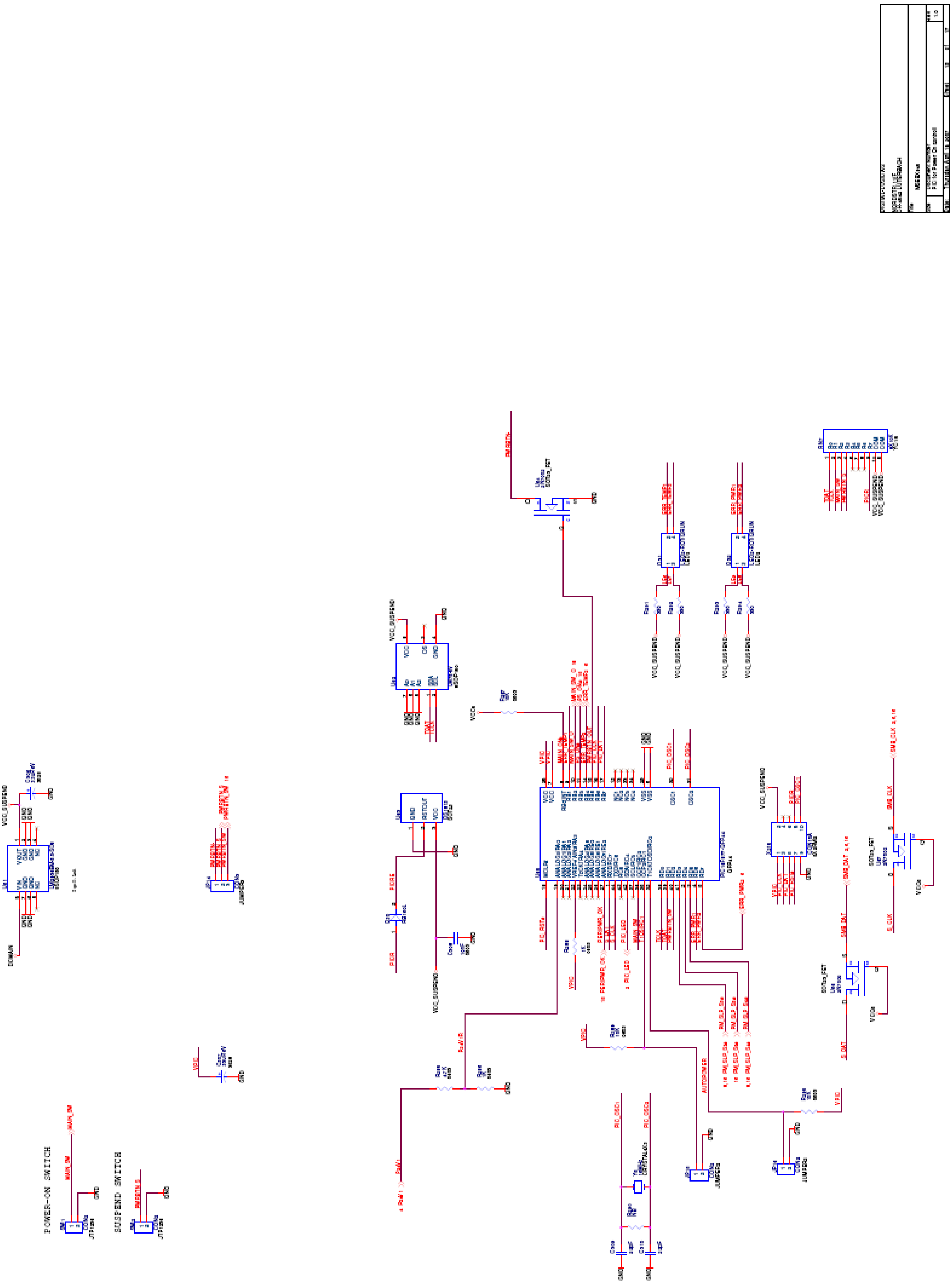


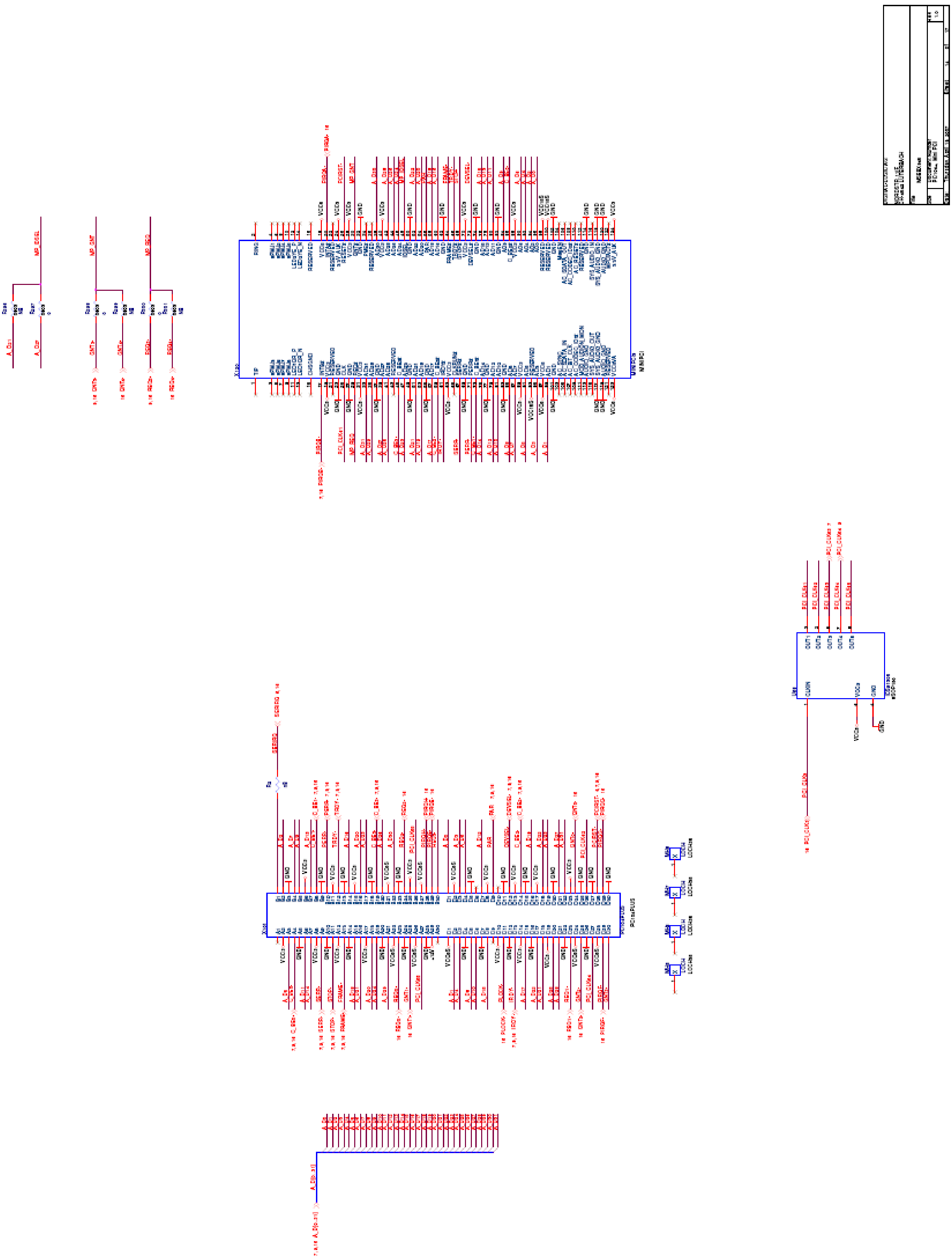


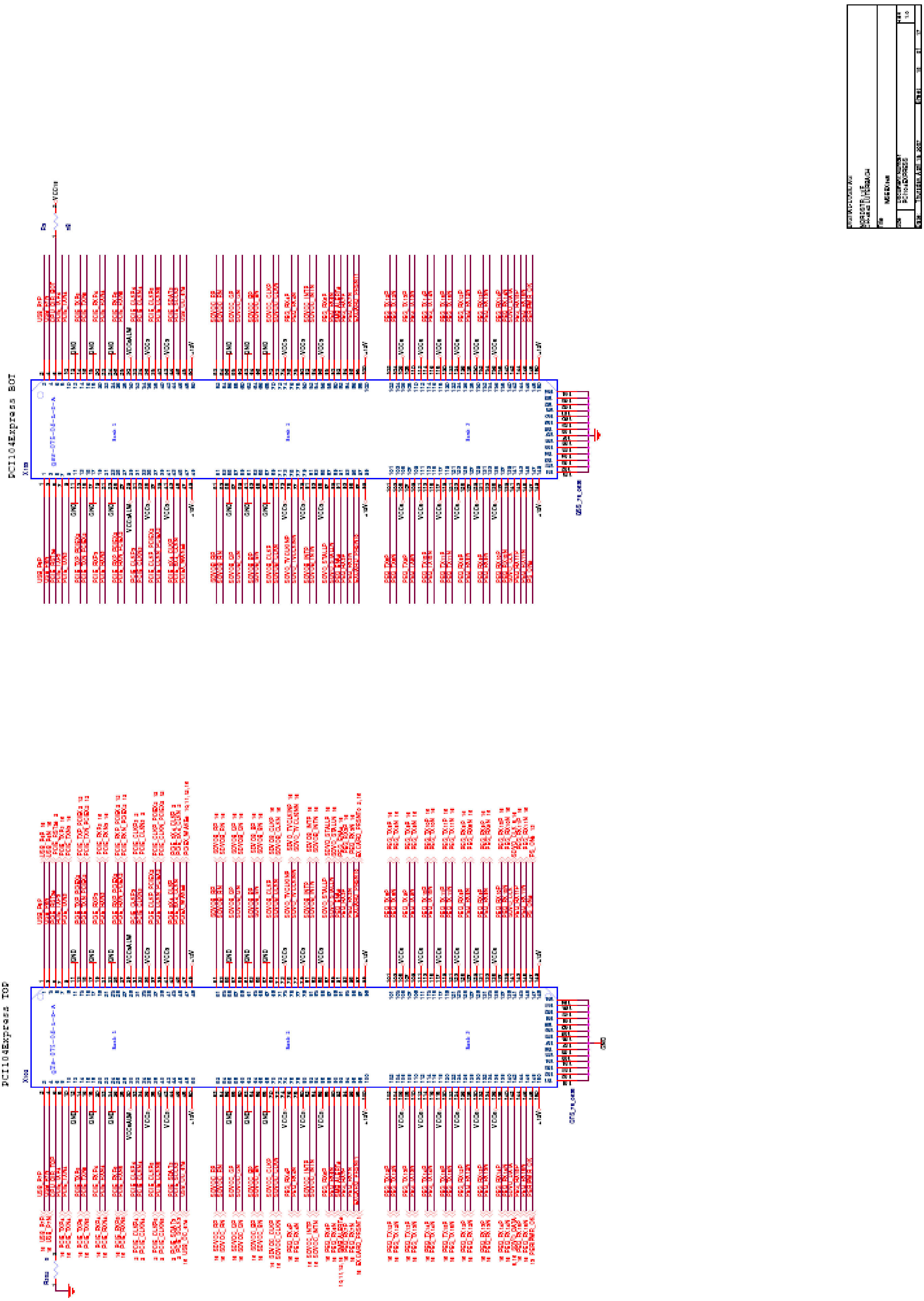


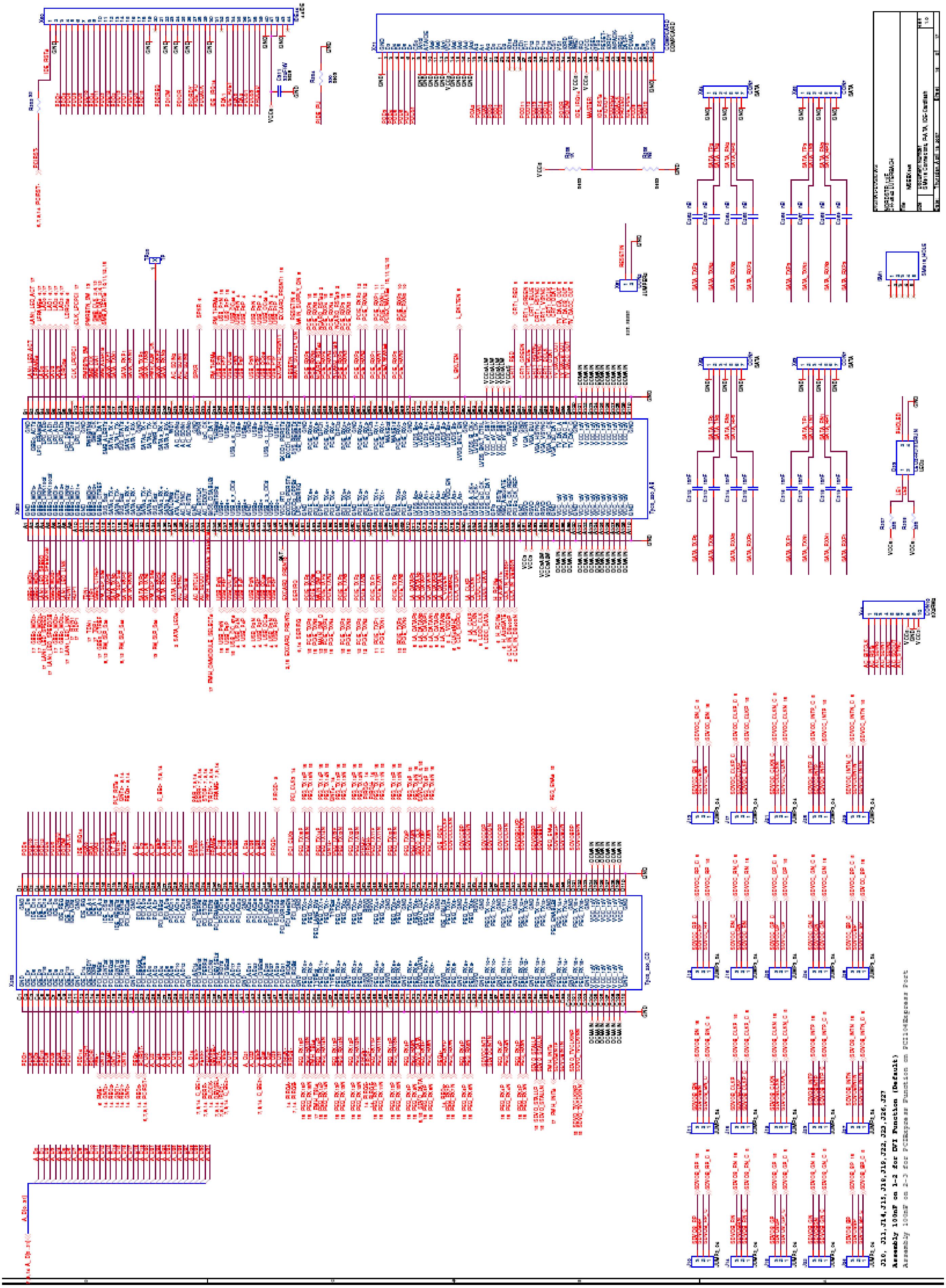


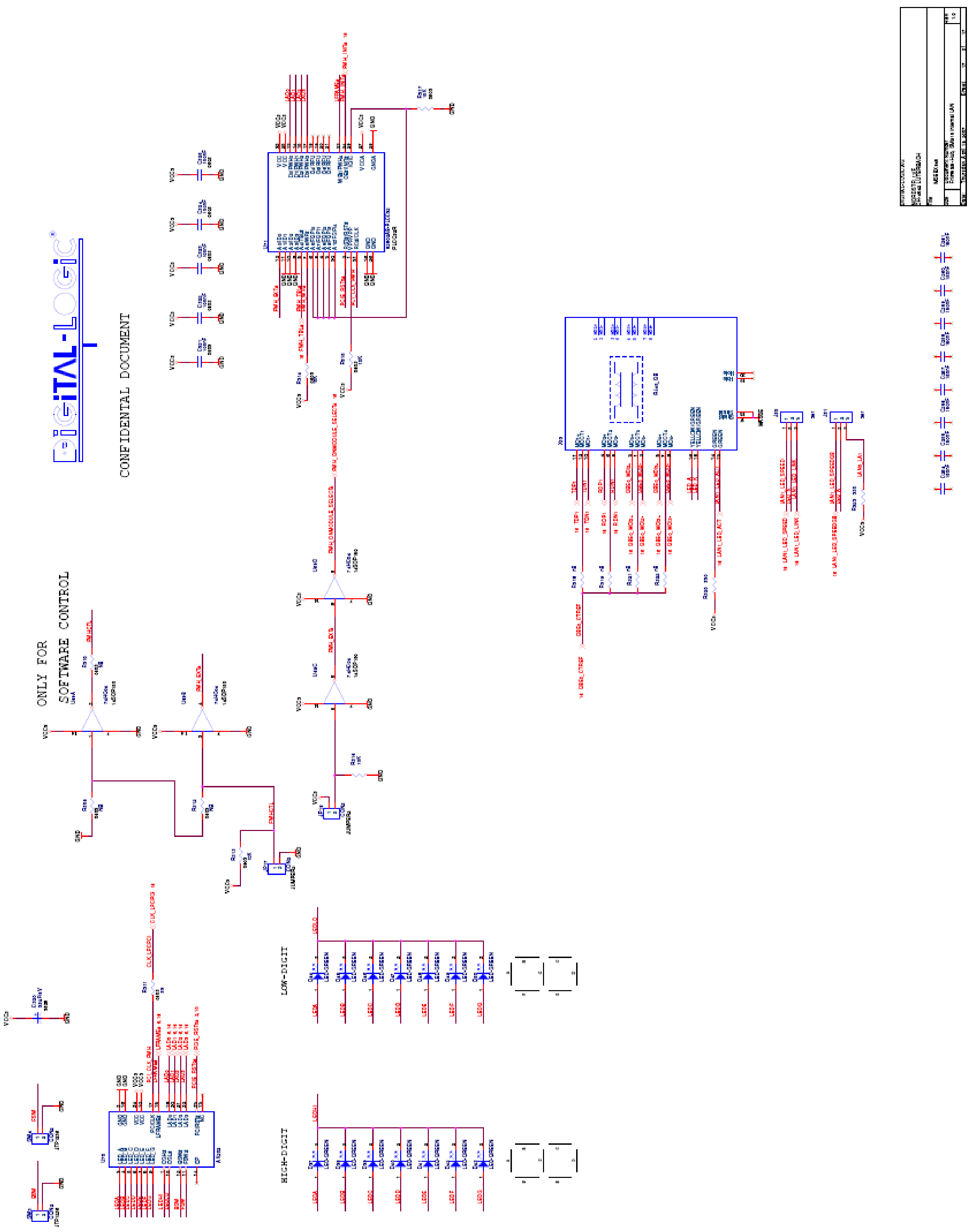







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11. INDEX

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